Cray Research ATM Development

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ABSTRACT: *This paper outlines Cray Research's development history using Asynchronous Transfer Mode(ATM) Technology, development direction for higher rates of ATM and how ATM will be incorporated with the Gigaring Channel.*
Topics covered include ATM Technology and it's benefits, the development program, ATM platforms and vendors, ATM standards support, performance results, future ATM development direction and Gigaring Channel to ATM connectivity.

Introduction

Cray Research started it's ATM research and development program in late 1993. This decision was based on the benefits of ATM which would make it highly useful on Cray systems. In LAN environments; ATM provides a transparent media solution along with scalable bandwidth capabilities. For the WAN environment; the LAN/WAN barrier is eliminated allowing for high speed circuit based worldwide connectivity. Multimedia applications will also benefit by the simultaneous transfer capabilities of audio, video and digital data traffic. Also, global support for ATM by the present standards bodies validated Cray's prerequisite to offer standards based interfaces for Cray customers.

ATM Development Program

At the start of the development project, it became clear that the best way to learn about ATM and offer an implementation on Cray systems with the best performance, was to get Cray customers also interested in this new technology to join in the development.

The pilot program started in mid 1994. Selected partners were able to connect Model-E based Cray systems to an ATM interface via a HiPPI channel on the model-E and Cray's Bus Based gateway(BBG). A BBG is a Sparc based platform that has a HiPPI and a single ATM interface. On Entry Level(EL) systems, an integrated VME solution was used. Through the remainder of 1994 tuning and code enhancements were made.

In 1995 the upgrade from TAXI to OC-3 SONET/SDH was made. The integrated VME ATM was incorporated into the J90 system and the ATM feature software was applied to UNICOS releases.

ATM Platforms and Vendors

For 1996, Cray has the Bus Based Gateway(BBG) and the integrated VME ATM interface as products. The ATM interfaces used in these products are from INTERPHASE Corporation. FORE Systems interfaces have also been used extensively in the development of Cray's ATM product offerings.

ATM Standards Support

The Internet Suite is the basis for connectivity with Cray systems. Cray supports the UNI 3.1 standard and the applicable Internet Engineering Task Force(IETF) Request For Comment(RFC's) which deal with ATM support over TCP/IP.

RFC 1483 - Multiprotocol Encapsulation using Logical Link Control(LLC's) or Virtual Circuit(VC) based. Cray supports the TCP/LLC portion of this RFC.

RFC 1577 - Support for 802.2 headers and ARP.

RFC 1626 - Provides for the default MTU value of 9k.

RFC 1755 - Specifies requirements for signaling support for IP over ATM.

All applicable ATM standards support is now incorporated into UNICOS at release levels 8.0.4 for the integrated VME product, and 9.0 for the Bus Based Gateway(BBG) product.

ATM Performance

Performance of the Cray ATM interfaces have increased steadily as software and hardware improvements have been made through the development program.

Using the initial TAXI based ATM interfaces, a rate of 65Mb/s using 9K MTU was sustained with an Entry Level(EL) system. The Bus Based Gateway(BBG) had a rate of 90Mb/s using 65K MTU.

Moving from TAXI to SONET OC-3(155Mb/s rated, 140Mb/s payload) took the performance of the EL system to 76Mb/s and the BBG to 100Mb/s. Using 9K and 65K MTU's, respectively.

The next progression in throughput came from moving from the EL platform to a J90 platform. Coupled with software improvements, the rates increased to 100Mb/s with the J90 and 110Mb/s with the BBG. Again, with the same 9K and 65K MTU's, respectively.

At this point in the development program, multiple interface testing began. Using an 8 processor J90 with seven VME-ATM interfaces connecting to SGI and SUN workstations. A sustained rate of 86Mb/s (9K MTU) per interface was achieved. For the BBG, a YMP-E system with 4 BBG's attached to 4 EL systems were used. a sustained rate of 100Mb/s (65K MTU) was attained. It should be noted that 4 BBG's is not a limiting factor but, rather how many HIPPI interfaces can be attched to the I/O subsystem. At the time of the testing, only 4 were available. **All performance testing was done using the nettest application which does memory to memory transfers using TCP/IP.**

As noted, the VME based ATM interface was not capable of handling MTU's larger than 9K. This restriction has recently been removed and it's expected that another performance gain for the VME based ATM interface will be realized.

All of the performance achieved to date was accomplished with FORE Systems ATM interface products.

In recent months, initial testing and acceptance of INTERPHASE Corporation VME and SBus based ATM interfaces was completed. Although complete performance results are not yet available, initial single stream testing of the VME based interface attained 115Mb/s.

Second generation interface cards are either available or soon to be available. These interfaces have improvements in on board buffer capacity and refinements in managing the Protocol Data Unit(PDU) as well as support for upcoming features in the UNI 4.0 specification. It is anticipated that another performance gain will be achieved in the area of 120-130Mb/s with the present OC-3 SONET based interfaces.

Future Development direction

Continuing development direction will encompass evaluating INTERPHASE and FORE Systems second generation Network Interface Cards(NIC's) to boost the performance of Cray's OC-3 products.

Compliancy testing of Q.2931 signaling software. This software was written based on UNI 3.1. Prior to release it will include UNI 4.0 provisions.

Support for UNI 4.0 will be implemented as it relates to Cray's Internet suite and to the features that will be supported by the hardware vendors.

OC12 development plans are to integrate the anticipated Sbus product from SUN Microsystems into Cray's product offering for the Gigaring Channel connection. Availability of the OC12 interface from SUN is anticipated to be in 1996.

A Cray OC48 design is being researched to determine what the requirements are that Cray customers would need in an OC48 interface for. This will determine what the design should encompass. e.g. number of VCI's, buffering capacity and other issues.

GigaRing Channel and ATM

Cray's GigaRing Channel offers dual ring access at rates up to 600MB/s per ring for an aggregate of 1.2GB/s. Connected to the Gigaring will be a Multi Purpose Node(MPN). The MPN is an SBus based platform that uses industry standard interface cards. Ethernet , FDDI and ATM OC-3 are supported

Upon OC12 Sbus interface availability. It will be integrated into the MPN and is expected to be available first quarter 1997.

OC48 plans will call for a Single Purpose Node(SPN). The SPN is an interface specific design which will plug directly onto the GigaRing Channel.

No dates have been set for OC48 prototyping.