

Acceleration technologies for high-performance computing



CRAY Users Group - May 2007

About DRC

- ▶ Announced OEM relationship with Cray in May 2006.
- ▶ Programmable coprocessors for compute-intensive applications
- ▶ Complete development platform for developing accelerated applications



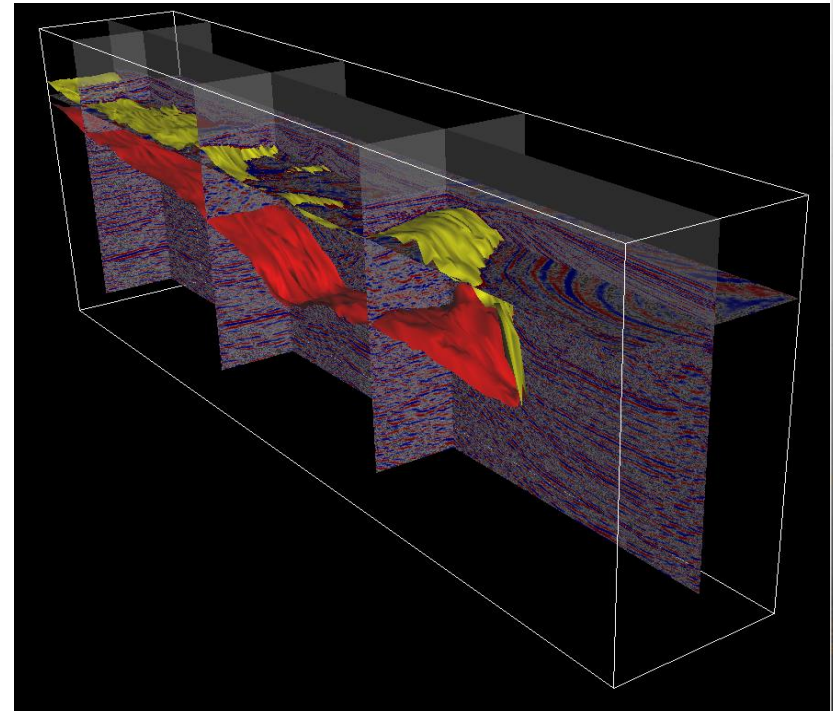
Real Customer: 3D Seismic Imaging

▶ **Creating this visualization using traditional microprocessors required:**

- Terabytes of data
- 1000's of processors
- Months of computing

▶ **The DRC RPU™ system:**

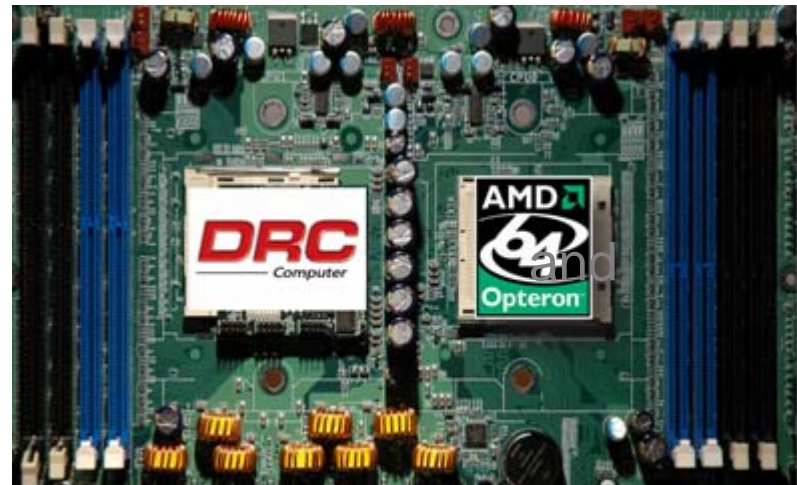
- 5X node count reduction
- Save 85% on utility bill
- Less than half the cost of non-accelerated solution



Data courtesy of Unocal

DRC Leverages Standard Technology

- ▶ Provides a standard programming environment
- ▶ Leverages world-class processors, memories, and motherboard technology
- ▶ Uses world-class FPGAs
- ▶ Enables quick response to standards changes:
 - Upgradeable software
flexible hardware
 - High performance
 - Fast time to market

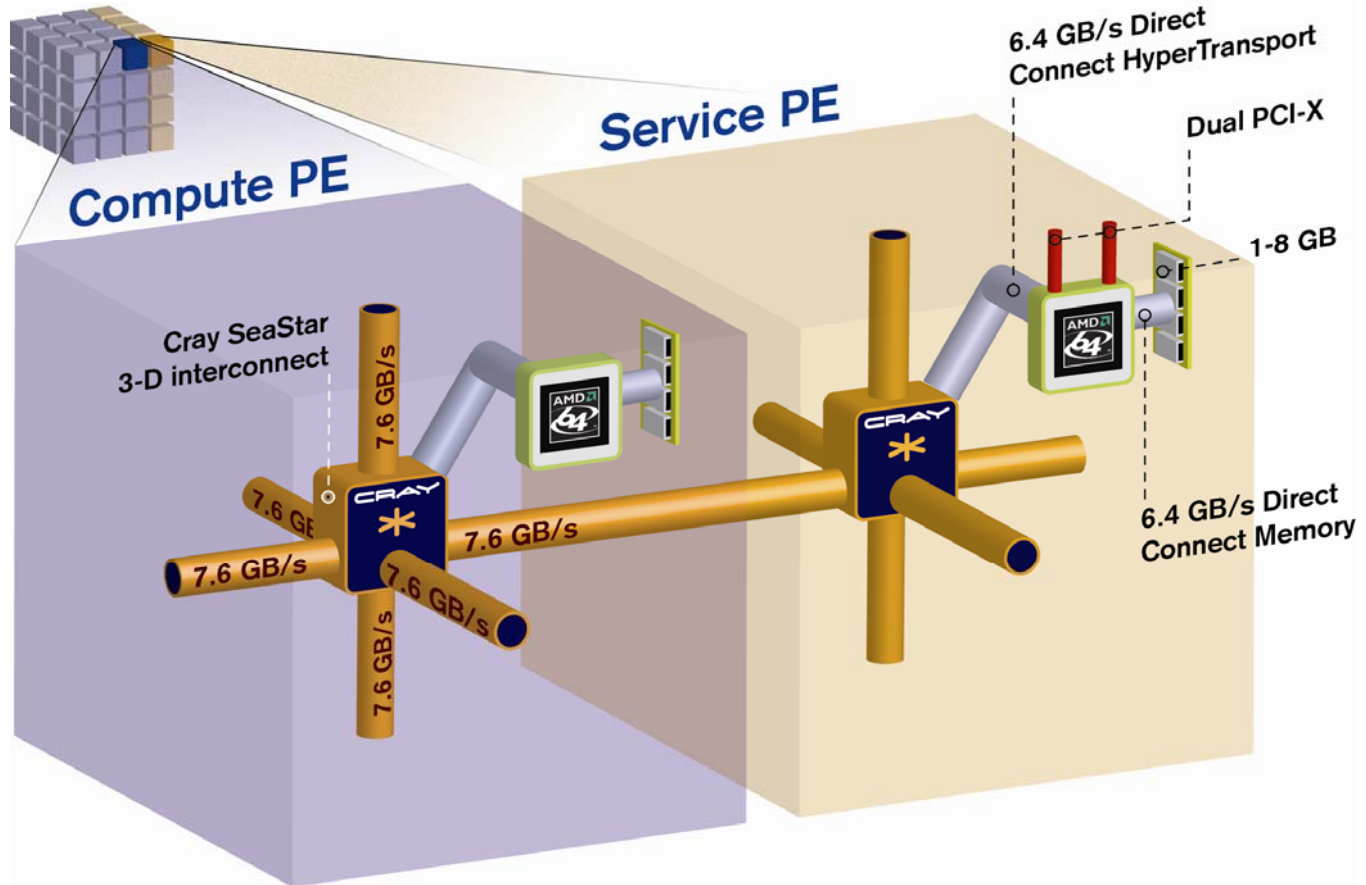


RPU110 -L200: The most powerful coprocessor available

- ▶ Largest FPGA available
- ▶ Most memory available (8.1GB)
- ▶ Highest memory BW (10.6GB/s)
 - 8GB DDR1 (motherboard, 6.4GB/s)
 - 8GB Opteron memory (1.6GB/s)
 - 128MB RLD-RAM (2.3GB/s)



CPUs and RPU - peers on a fast interconnect.

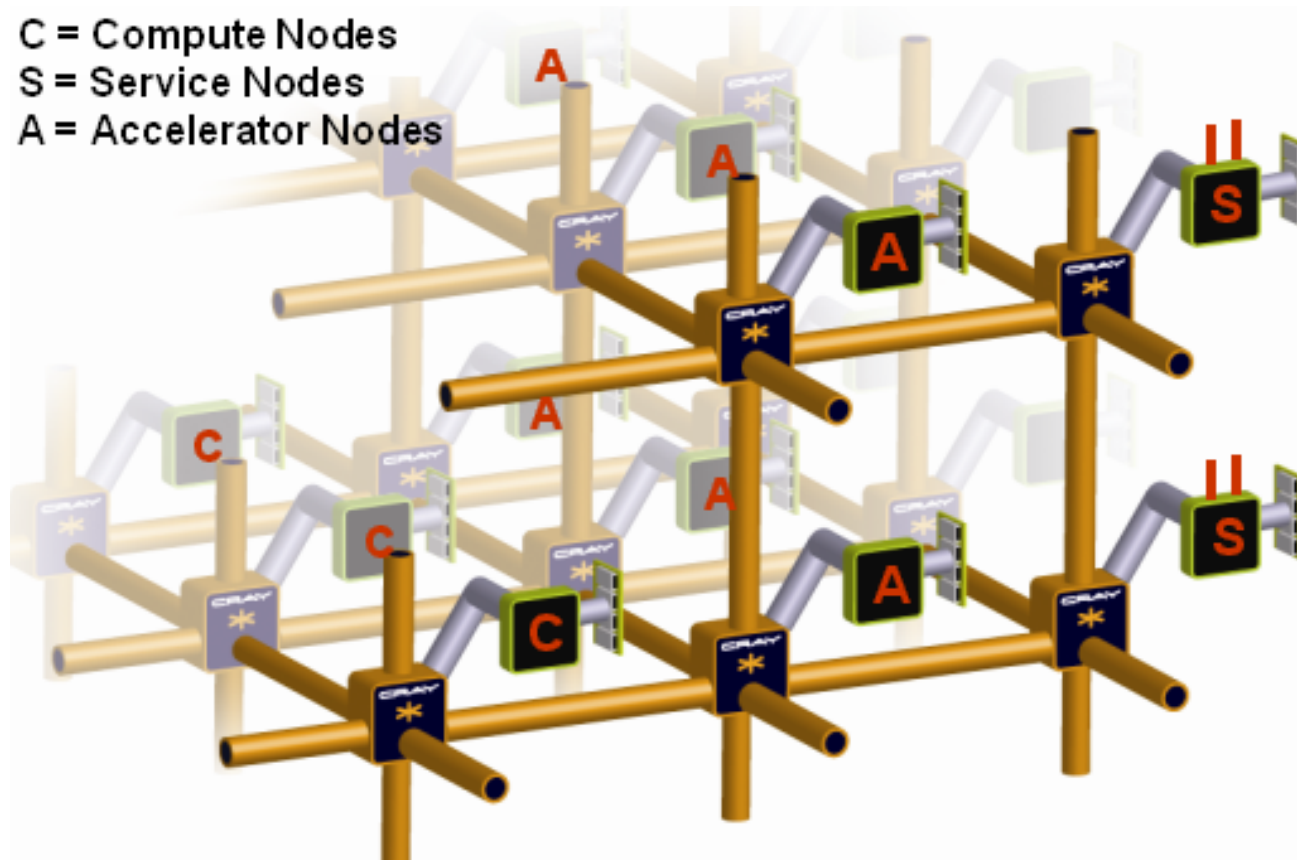


The Heterogeneous mix of nodes

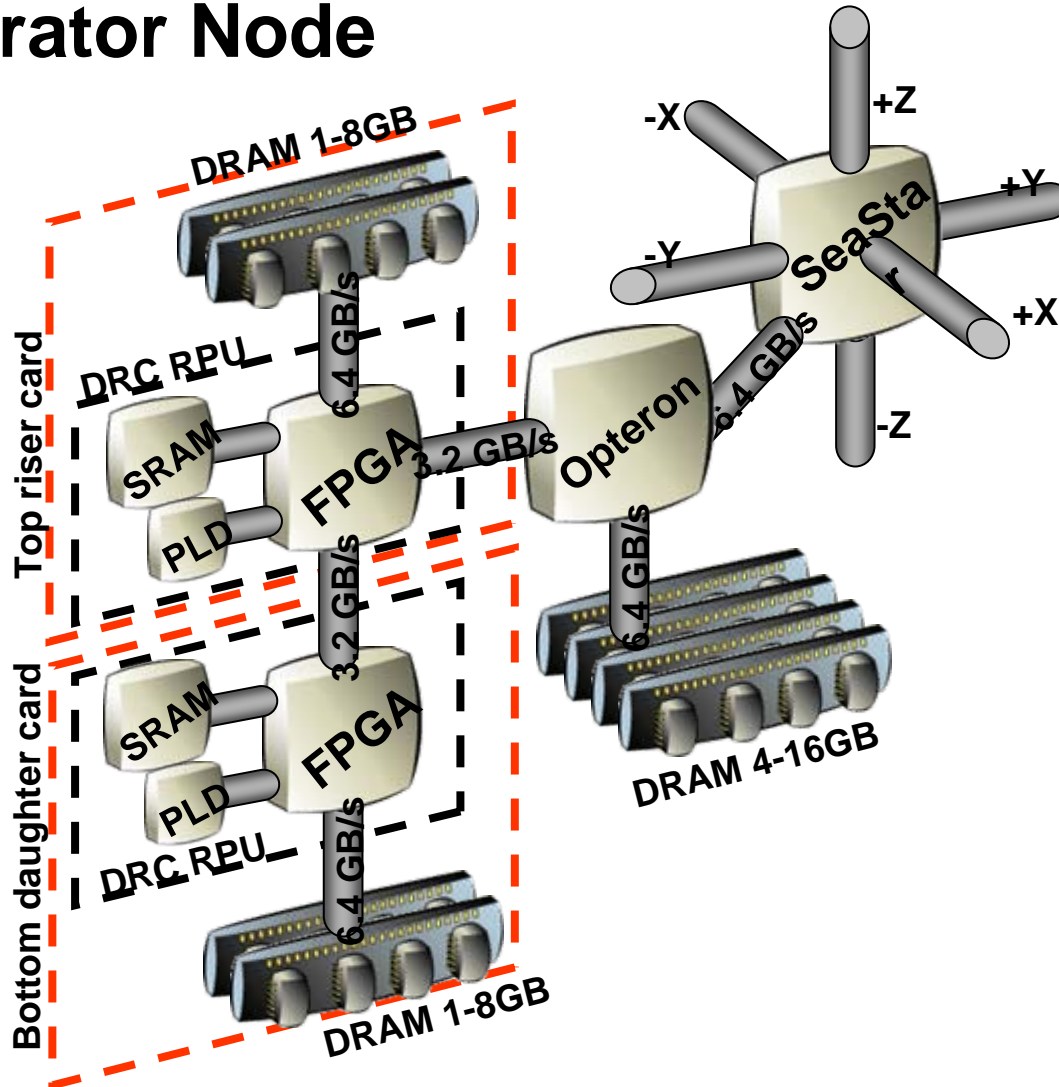
C = Compute Nodes

S = Service Nodes

A = Accelerator Nodes



Accelerator Node

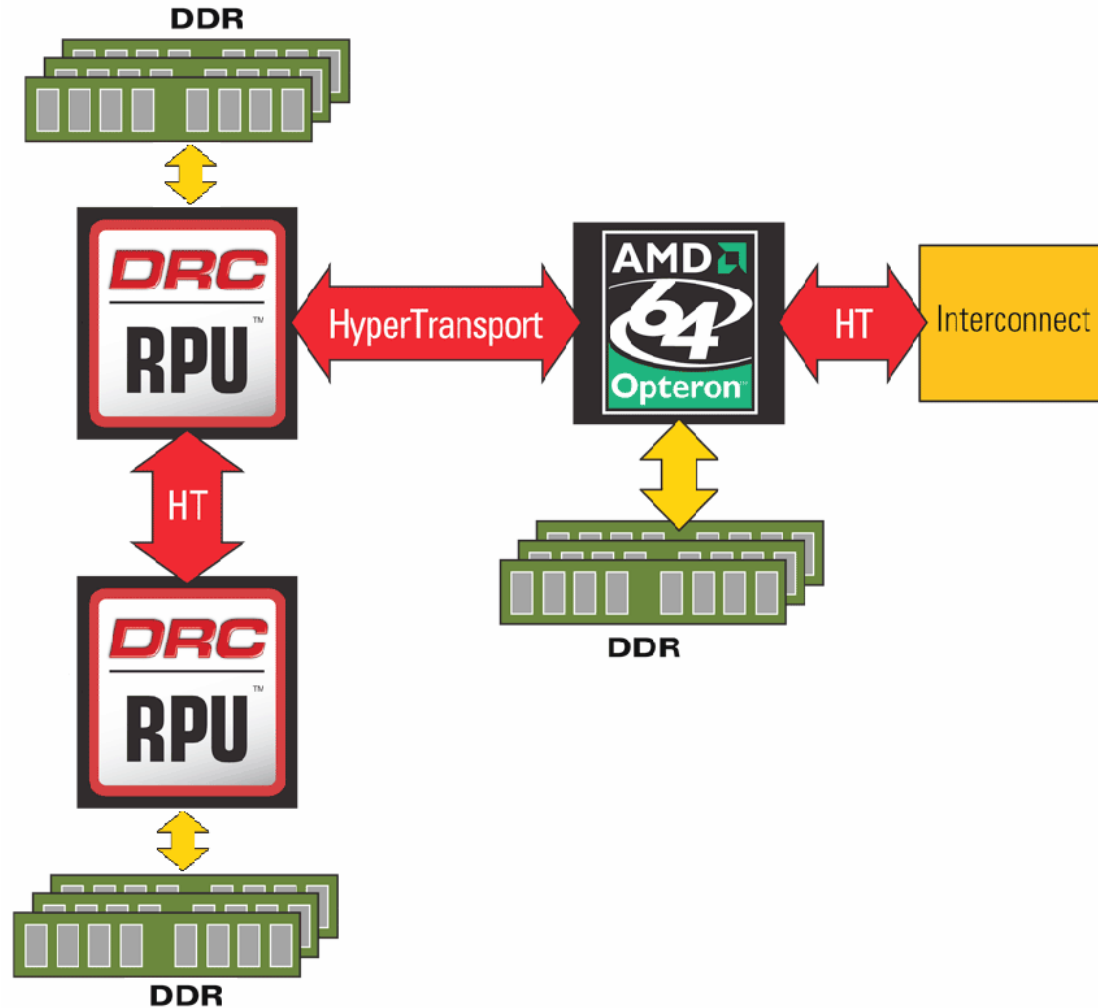


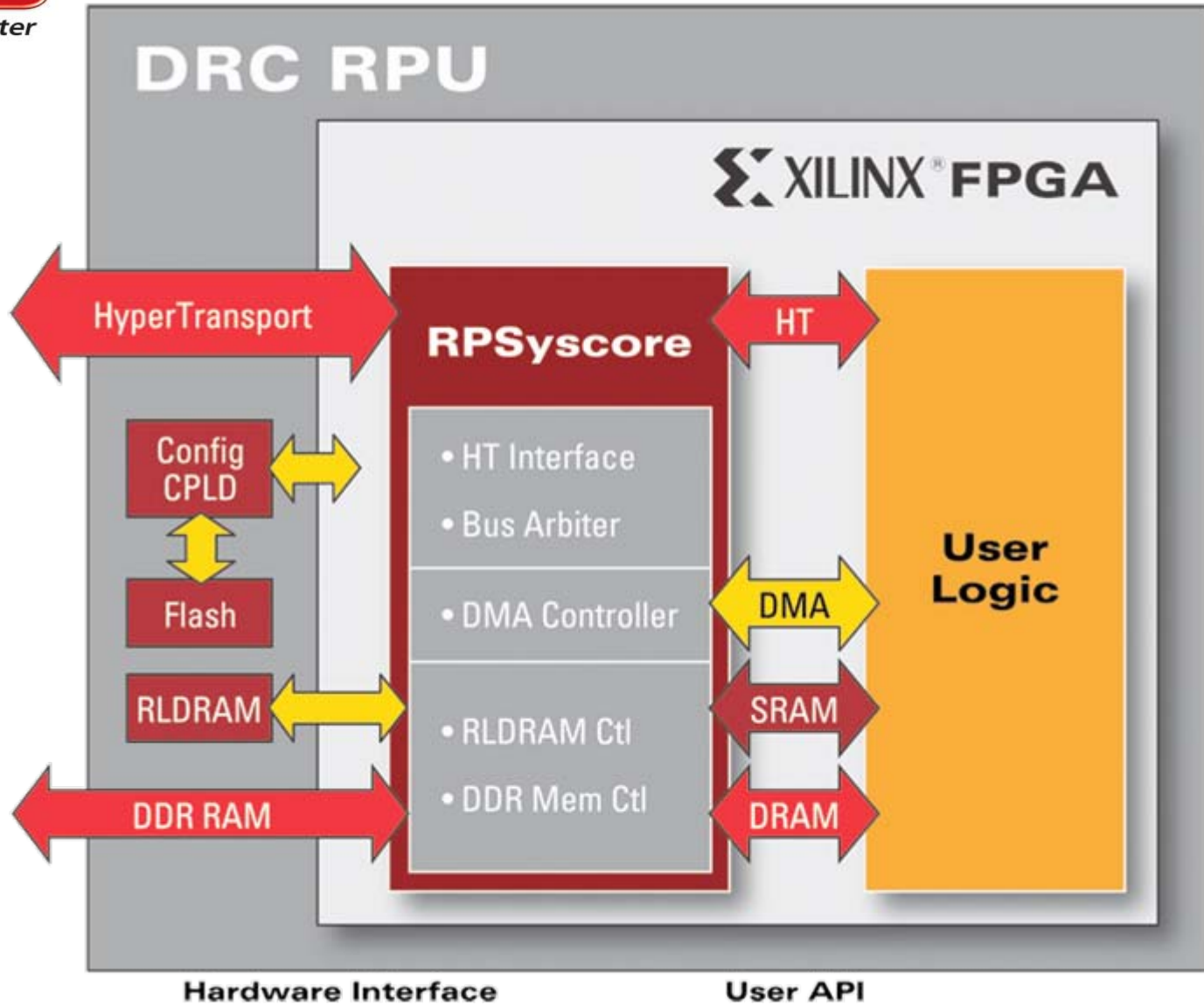
Development Systems for Cray XT supercomputers

The DRC DS/XT is a complete development platform that contains everything you need to get started modifying your application subroutines to run in Cray XT computer systems.



Accelerator PE = DS/XT Node





Complete Solutions Partners

▶ Development tools

- Celoxica 
- DSP Logic 
- Impulse C 
- Mitronics 
- Synplicity 
- Xilinx 

▶ Products and services

- Celoxica (UK) 
- Synective (Sweden) 
- XISS (Houston, TX) 
- XLBiosim (Switzerland) 

Typical Project Flow

- ▶ **Analysis & Design – 2-3 man-months**
 - Architect the application for fine-grained parallelism
 - Choose an implementation strategy (partners, tools etc.)
 - Estimate project time and cost

- ▶ **Prototype: 3-6 mm to simulate, port and verify**
 - Simulate for size, performance, function
 - Design and develop firmware
 - Bring-up prototype RPU and system

- ▶ **Production: 1-2 months to validate, stage and install**



Support:

▶ DRC for all support contact

- H/W
 - In conjunction with OEM supplier
 - Remote, 24 hour replacement
- S/W
 - RPU S/W by DRC
 - Tools with tool vendors help

Make it work for you

▶ Get your development done:

- Without burning cycles on the main supercomputer
- Supports scientists need to experiment
- Identical configuration of H/W node and MPI
- Affordable as a personal “unshared” platform

▶ A simple as possible today

- RPSysCore simplifies physical interfaces
- Tools provide best-in-class choices
- Documentation includes:
 - Quick start guide
 - Descriptions and glossaries
 - Tutorial examples

Questions?

Availability

- ▶ Offered through Cray or through DRC
- ▶ Availability:
 - Now in 2x2;
 - August 2007 for 1x2