The Effects of System Options on Code Performance

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Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

XT3 Available Options

- small vs. large pages
  - Controls memory page size
  - large pages are default
  - yod -small_pages ...
- eager vs. rendezvous message sends
  - Controls message protocol
  - rendezvous protocol is default
  - export MPI_PTL_EAGER_LONG=1
- Catamount malloc vs. GNU malloc
  - Controls which malloc is being used
  - Link time option (cc ... -lgmalloc ...)

Test Parameters

- Codes were run for all combinations of options
- Codes were run using only one core per socket
- All results on a given number of processors for a given code were run using the same nodes on the machine
- Most of the results are from Red Storm (2.4 GHz processors) while some are from our test system (2.0 GHz processors)
- Most tests were run once
  - Early experience with the test system indicated that this was sufficient

HPCC

- Series of 7 benchmarks in one package. We are using 5 of them:
  - PTRANS - matrix transposition
  - HPL - Linpack direct dense system solve
  - STREAMS - Memory bandwidth
  - Random Access - Global random memory access
  - FFT - large 1-D FFT
- Code is C plus libraries

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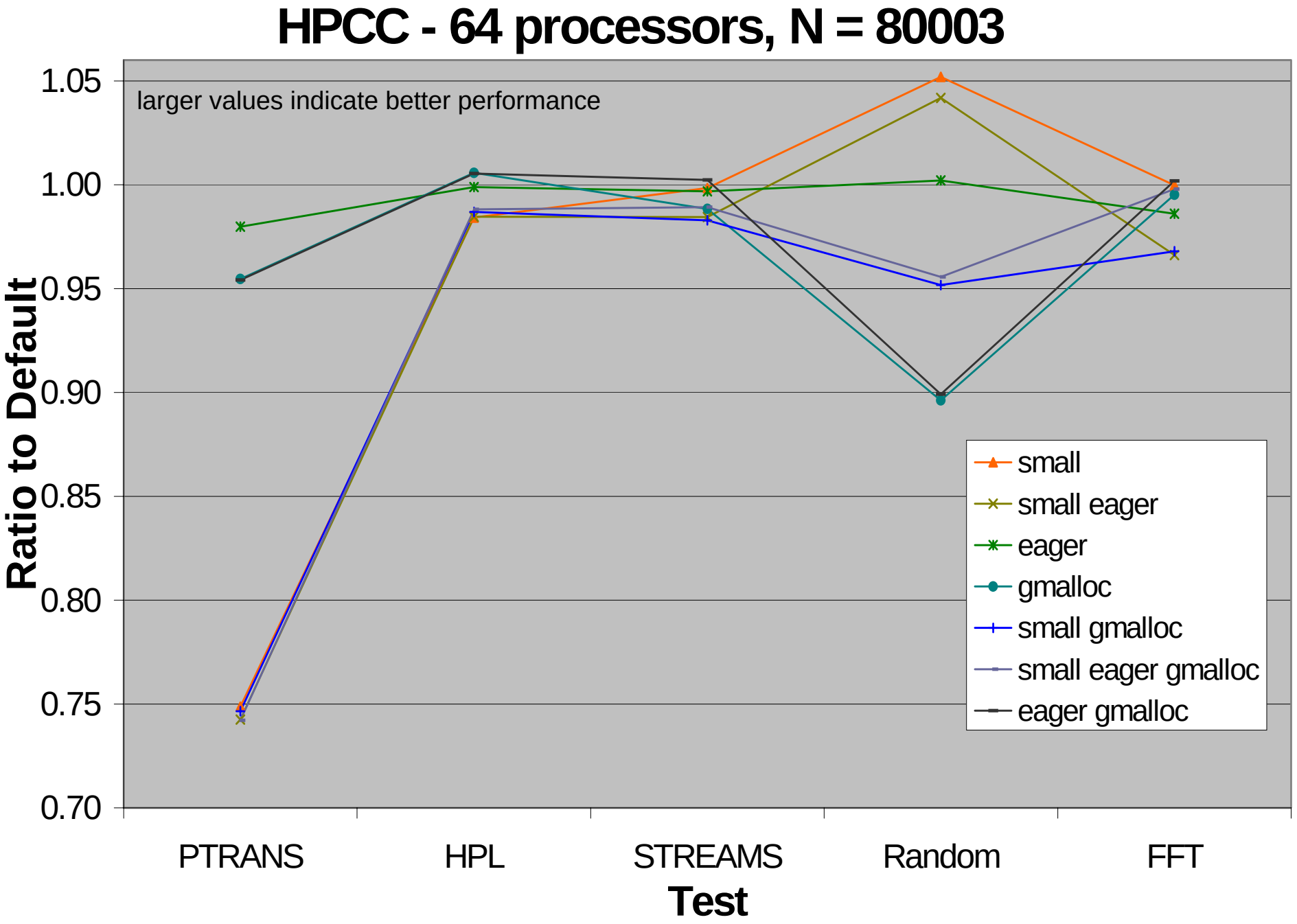
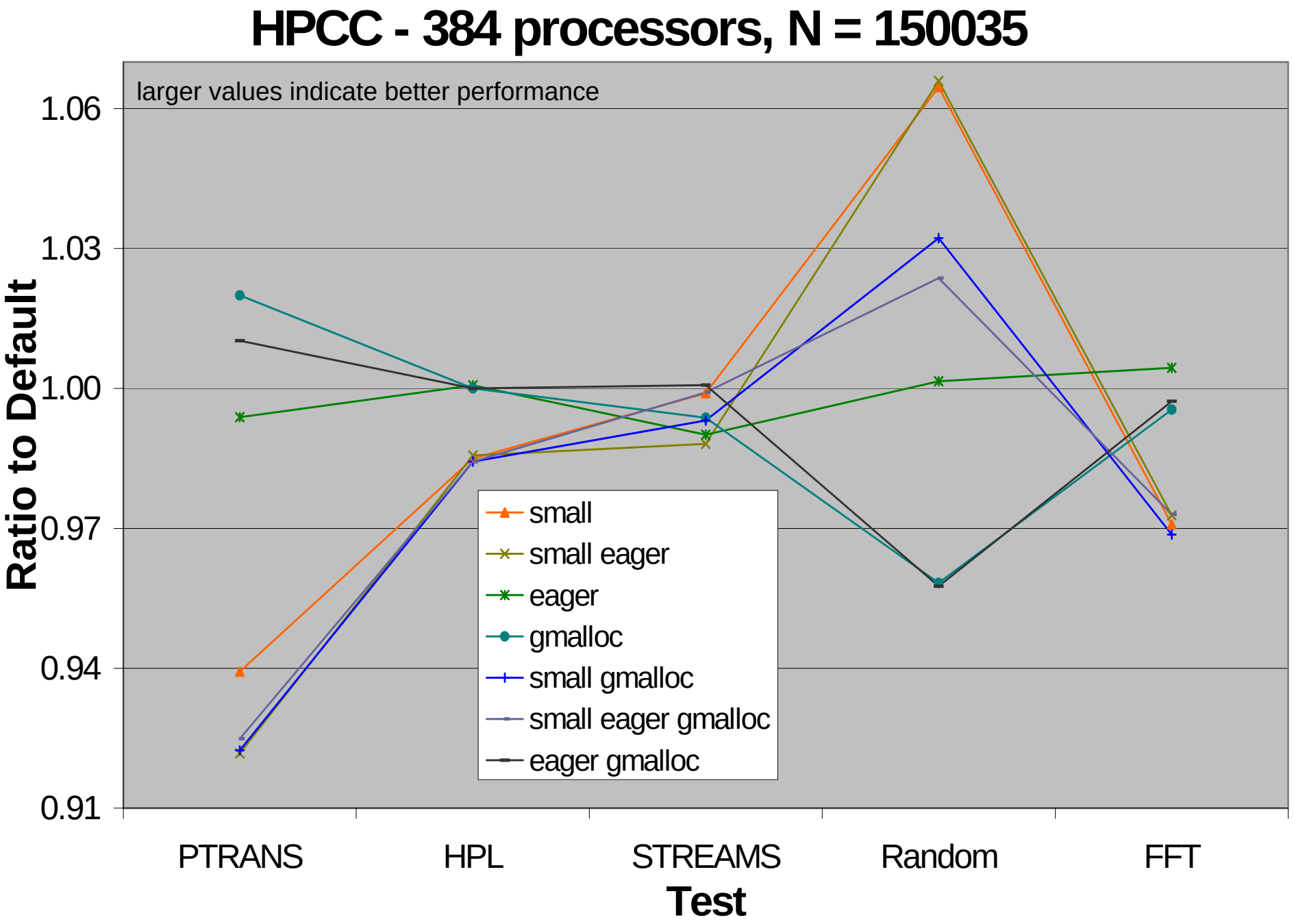
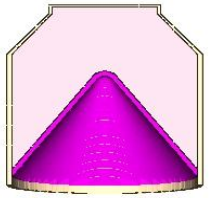

HPCC - 64 processors, N = 80003
larger values indicate better performance
Ratio to Default
1.05
1.00
0.95
0.90
0.85
0.80
0.75
0.70
PTRANS
HPL
STREAMS
Random
FFT
Test
small
small eager
eager
gmalloc
small gmalloc
small eager gmalloc
eager gmalloc

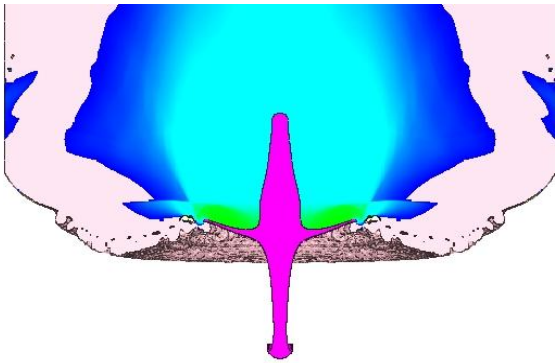

HPCC - 384 processors, N = 150035
larger values indicate better performance
Ratio to Default
1.06
1.03
1.00
0.97
0.94
0.91
small
small eager
eager
gmalloc
small gmalloc
small eager gmalloc
eager gmalloc
PTRANS
HPL
STREAMS
Random
FFT
Test

CTH

- **Three-dimensional shock hydrodynamics code**
- **Ran in flat mesh mode - no AMR (Automatic Mesh Refinement)**
- **Shaped charge problem**
- **90 x 216 x 90 cells per processor**
- **Code is mostly FORTRAN with a little C**



time = 0.0 ms



time = 0.3 ms

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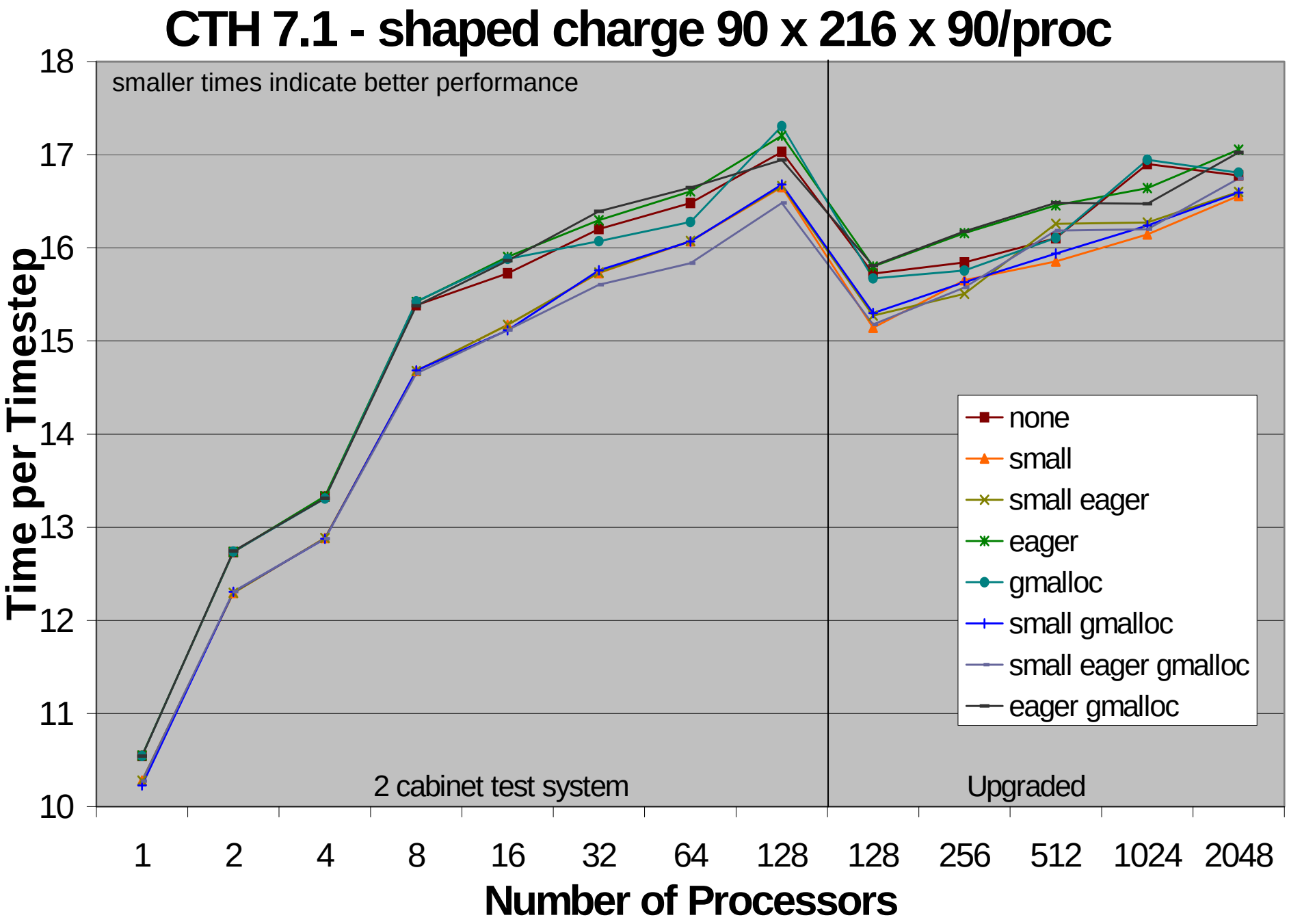
CTH 7.1 - shaped charge 90 x 216 x 90/proc
smaller times indicate better performance
Time per Timestep
18
17
16
15
14
13
12
11
10
2 cabinet test system
Upgraded
1
2
4
8
16
32
64
128
128
256
512
1024
2048
Number of Processors
none
small
small eager
eager
gmalloc
small gmalloc
small eager gmalloc
eager gmalloc

Partisn

- LANL code that solves the Boltzmann transport equation
- Has a transport and diffusion phase
- SN timing problem with 72^3 cells per processor
- Run only on 2 cabinet test system
- Code is mostly FORTRAN

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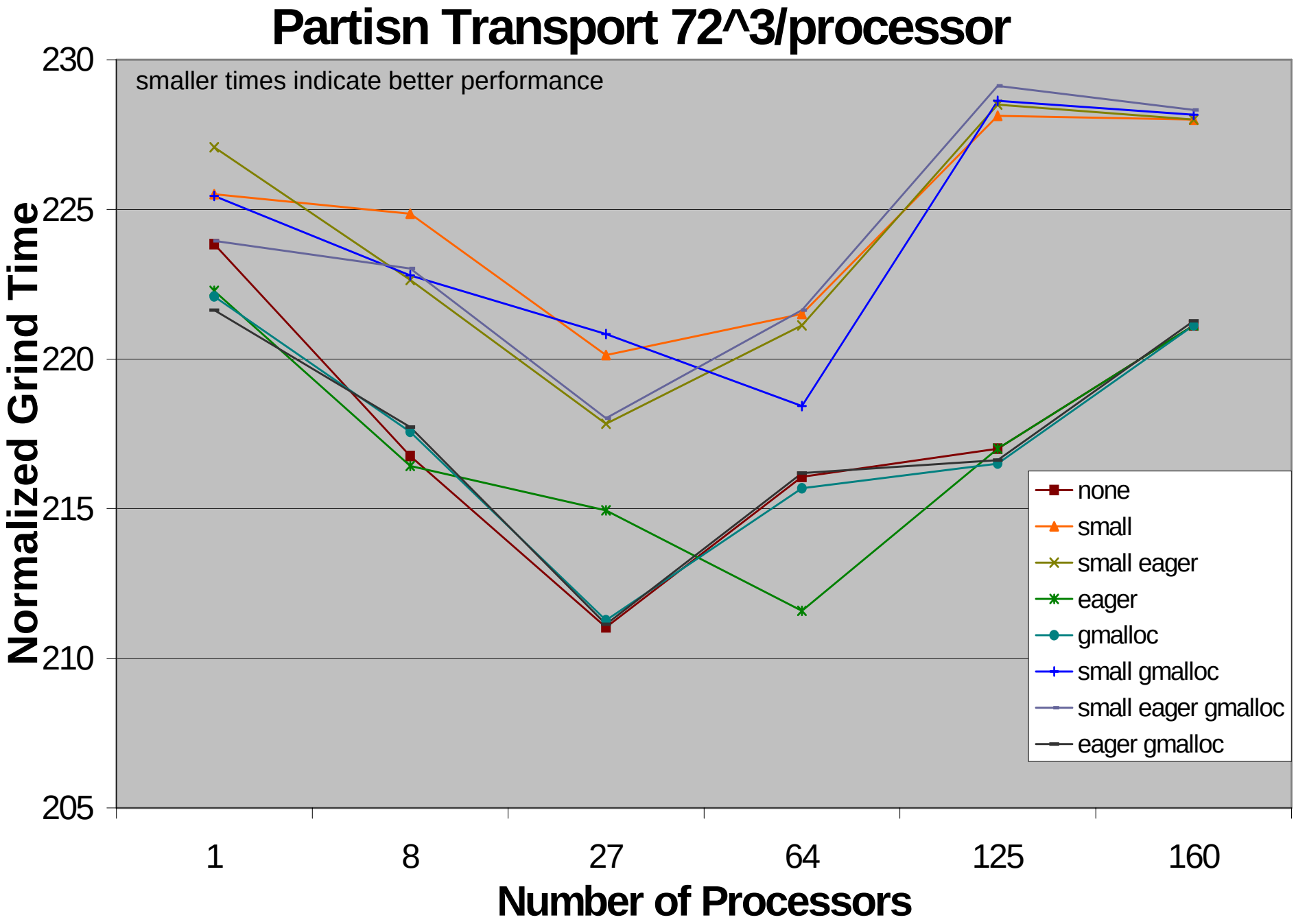
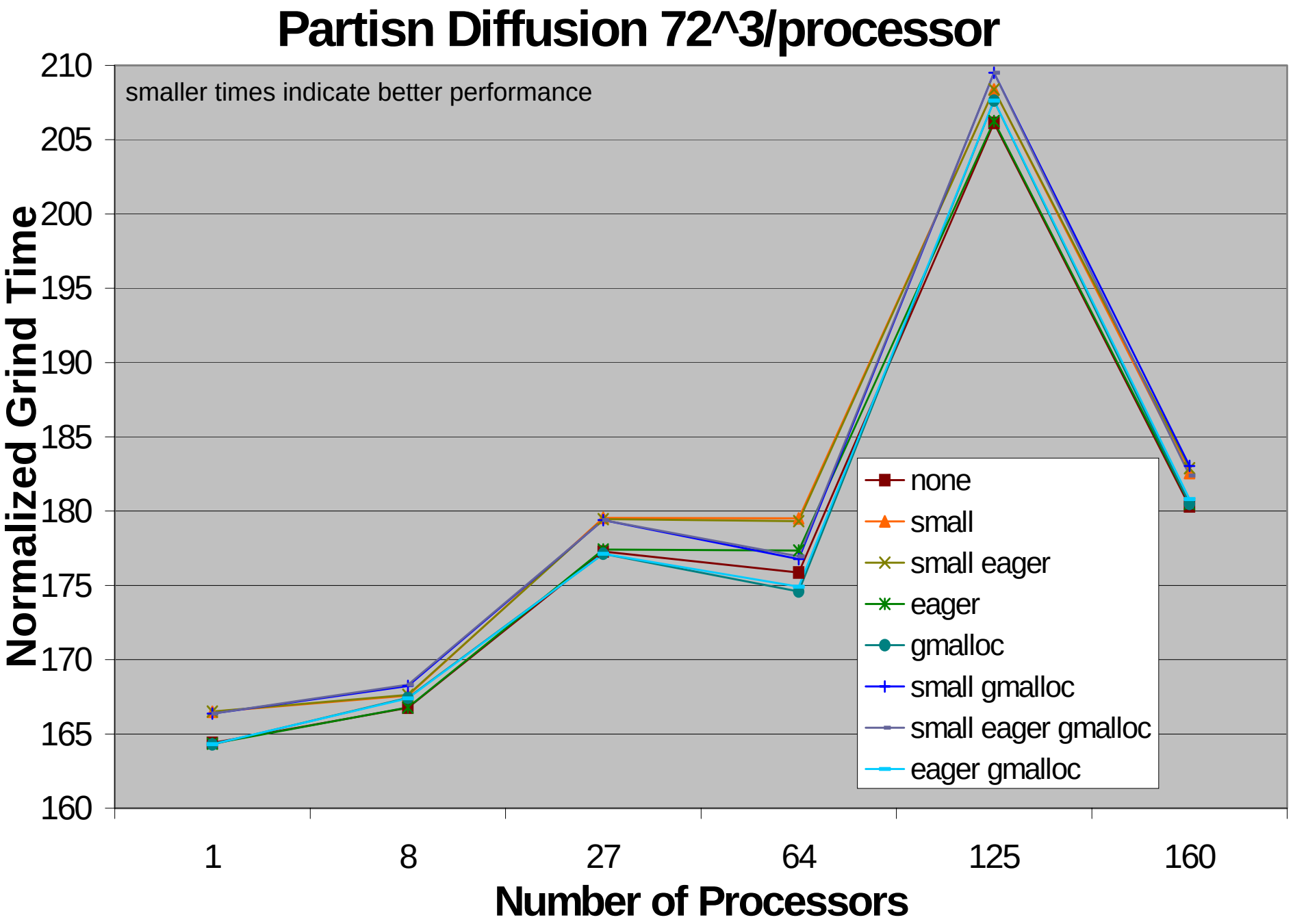
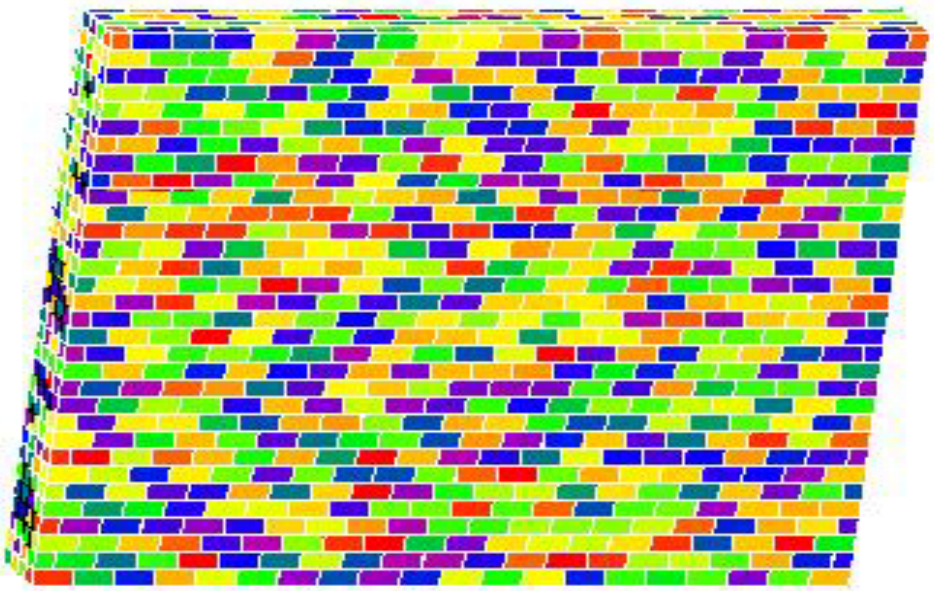

Partisn Transport 72^3/processor
smaller times indicate better performance
Normalized Grind Time
230
225
220
215
210
205
1
8
27
64
125
160
Number of Processors
none
small
small eager
eager
gmalloc
small gmalloc
small eager gmalloc
eager gmalloc


Partisn Diffusion 72^3/processor
smaller times indicate better performance
Normalized Grind Time
210
205
200
195
190
185
180
175
170
165
160
1
8
27
64
125
160
Number of Processors
none
small
small eager
eager
gmalloc
small gmalloc
small eager gmalloc
eager gmalloc

Presto

- Structural mechanics with contact algorithm
- Walls problem
  - Two sets of two brick walls colliding
  - 10240 elements/proc
- Each brick contained on a processor
  - All communication for contact
- Code is C++



32 processor problem
colored by processor number

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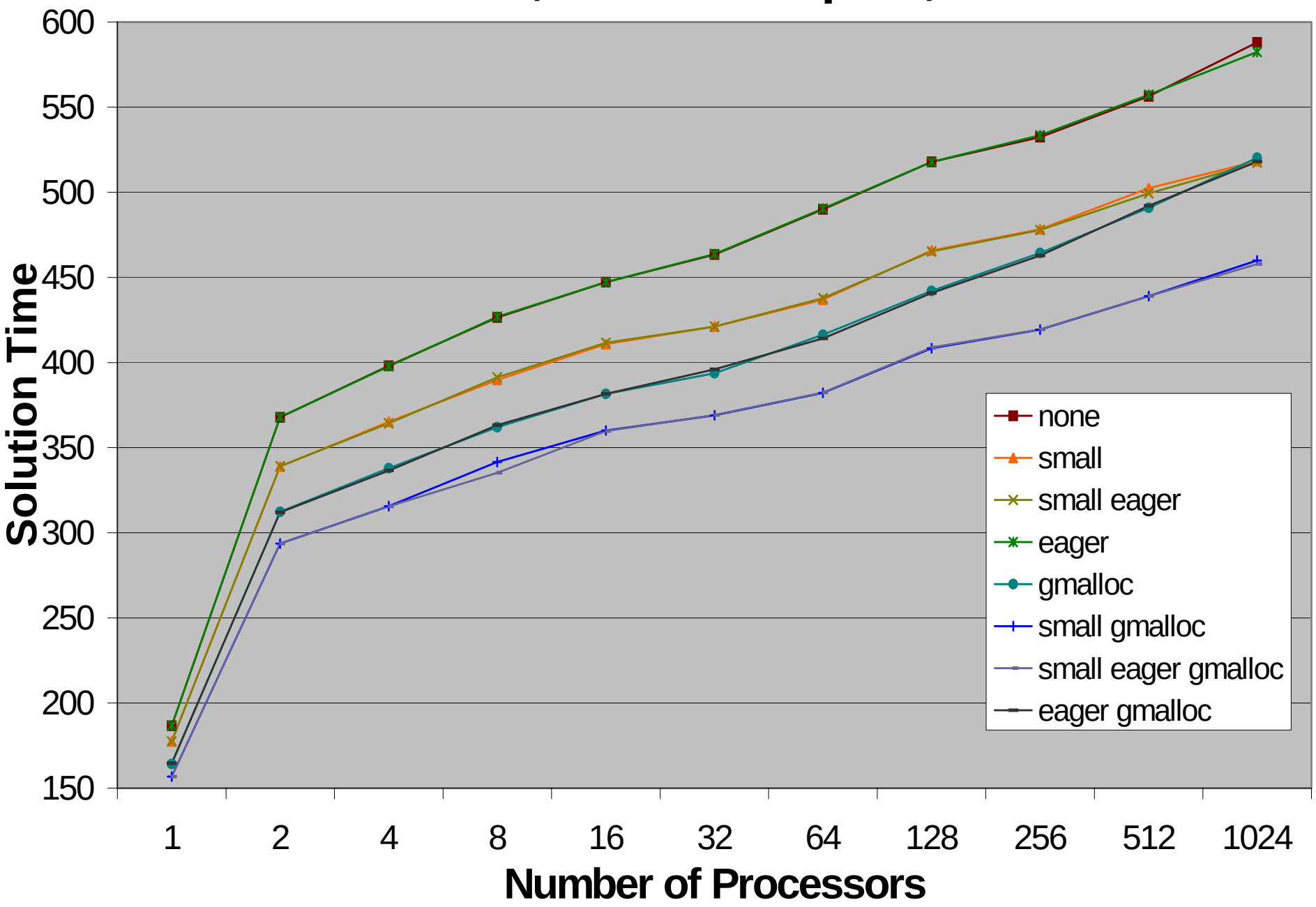
PRESTO - Walls, 10240 elem/proc, t = 5.0e-3
Solution Time
600
550
500
450
400
350
300
250
200
150
1
2
4
8
16
32
64
128
256
512
1024
Number of Processors
none
small
small eager
eager
gmalloc
small gmalloc
small eager gmalloc
eager gmalloc

SAGE

- LANL Eulerian Hydrocode with AMR (Adaptive Mesh Refinement)
- timing_c problem
  - has adaptation and heat conduction
  - 250000 cells per processor
- Code is mostly FORTRAN 90

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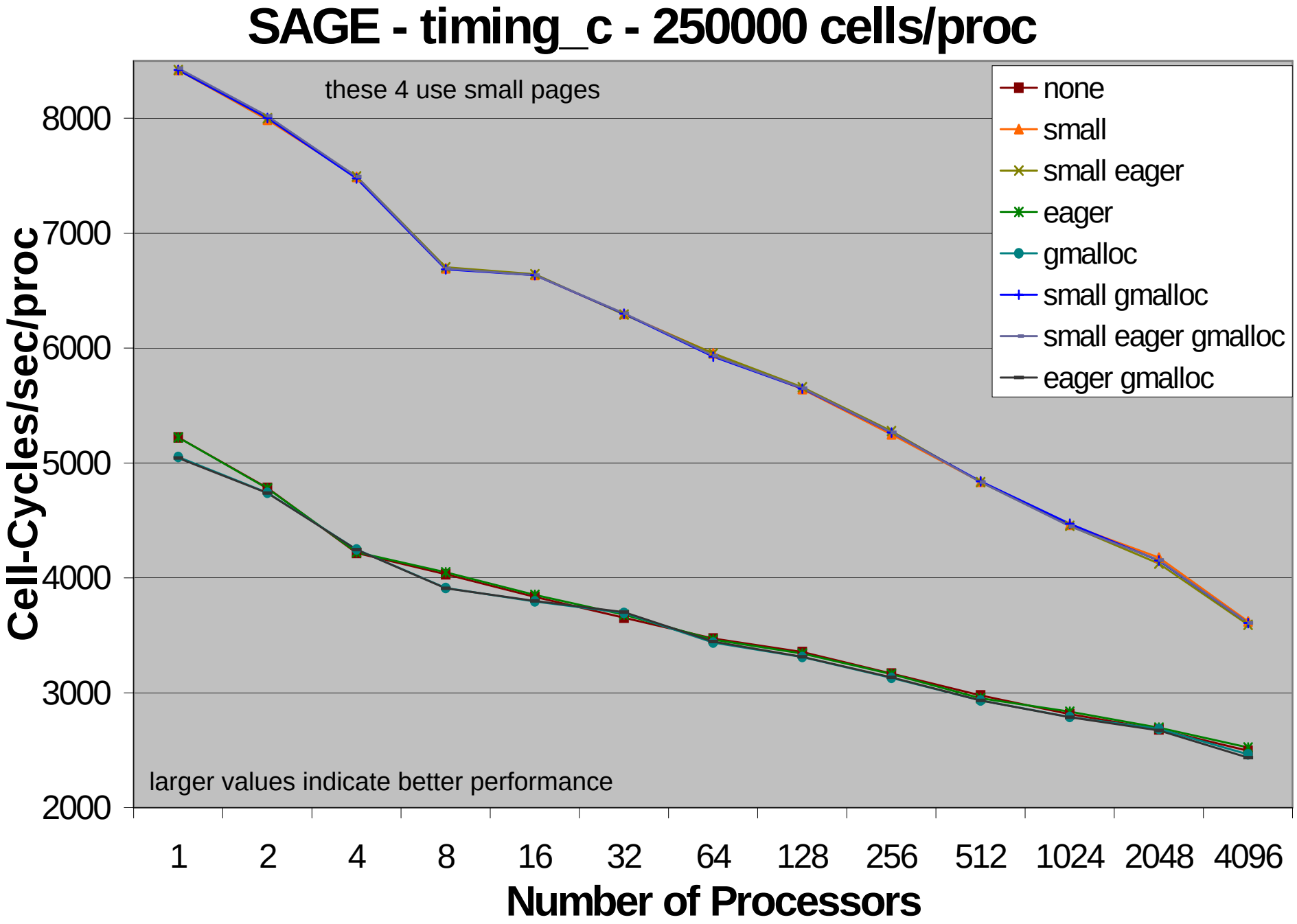
SAGE - timing_c - 250000 cells/proc
these 4 use small pages
larger values indicate better performance
Cell-Cycles/sec/proc
8000
7000
6000
5000
4000
3000
2000
1
2
4
8
16
32
64
128
256
512
1024
2048
4096
Number of Processors
none
small
small eager
eager
gmalloc
small gmalloc
small eager gmalloc
eager gmalloc

PAPI Results for Different Page Sizes

	Large pages					Small pages				
App	TLB miss	Cache access	Access /miss	Cache hit rate	FP intensity	TLB miss	Cache access	Access /miss	Cache hit rate	FP intensity
PTRANS	$3.30e^{7}$	$6.37e^{10}$	1934	98.2%	0.150	$1.03e^{9}$	$6.54e^{10}$	63.8	98.2%	0.144
HPL	$5.57e^{8}$	$3.16e^{12}$	5670	99.1%	1.693	$2.98e^{8}$	$3.17e^{12}$	10644	99.1%	1.686
PARTISN	$1.48e^{9}$	$6.14e^{11}$	414	92.8%	0.558	$1.38e^{9}$	$6.18e^{11}$	449	92.7%	0.554
STREAM	$1.73e^{4}$	$4.25e^{9}$	$2.45e^{5}$	93.5%	0.344	$6.97e^{6}$	$4.34e^{9}$	623	93.6%	0.333
FFT	$2.03e^{7}$	$3.34e^{9}$	164	97.6%	0.466	$1.52e^{7}$	$3.30e^{9}$	217	97.6%	0.441
CTH	$1.08e^{10}$	$1.28e^{12}$	119	96.9%	0.570	$3.30e^{9}$	$1.32e^{12}$	398	97.0%	0.588
Random	$8.50e^{8}$	$4.32e^{10}$	50.8	99.5%	0.0	$1.01e^{8}$	$4.57e^{10}$	452	99.5%	0.0
SAGE	$2.90e^{9}$	$1.29e^{11}$	44.5	98.7%	0.226	$2.29e^{7}$	$1.02e^{11}$	4457	98.3%	0.231

codes ranked by large page preference

Observations from PAPI Data

- The L1 data cache hit rate does not seem to change with different page sizes
- The floating point intensity of a calculation has no bearing on which page size is better
- The number of cache accesses per TLB miss can indicate something about which page size to use
- The number of L1 data cache accesses can vary with the page size

Summary

- No set of options is always best
- Results from benchmarks do not necessarily translate to codes
- Small pages generally helps and can help significantly
- GNU malloc helps C++ codes
- The eager message protocol has small effects for the codes that were tested

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