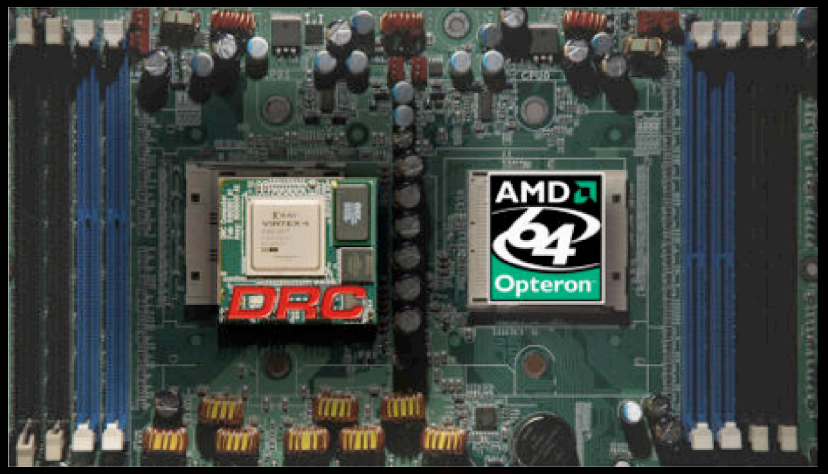
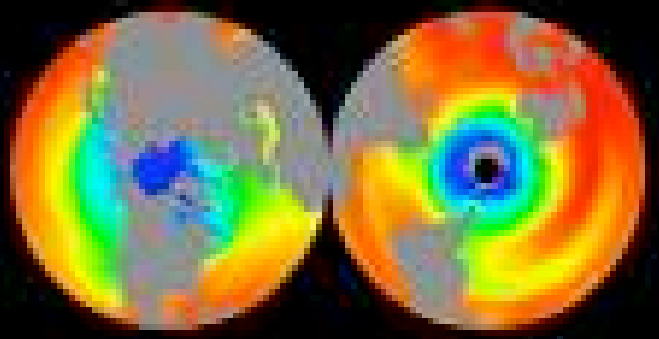
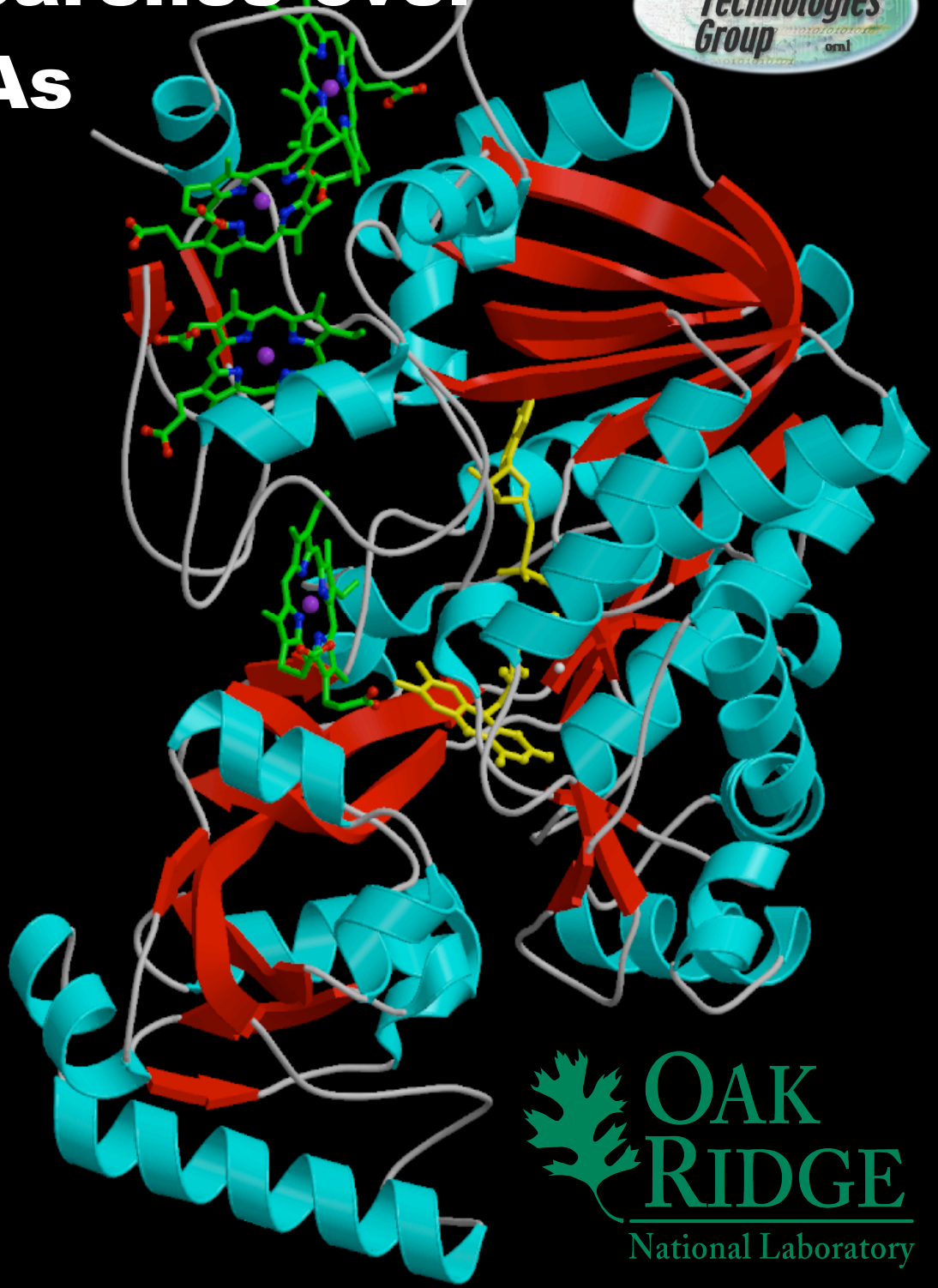
Speeding Genome Searches over 1000X with 150 FPGAs







Olaf O. Storaasli

Google **Olaf ORNL**

Cray Users Group '08 Helsinki

Future Technologies Group ornl

OAK RIDGE National Laboratory

Explore FPGAs for future ORNL HPC

HPC vendors adopting FPGAs

sgi

CRAY THE SUPERCOMPUTER COMPANY

Steve Scott, CTO HPCWire 24/3/0606

"*After exhaustive analysis, Cray concluded that, although multi-core commodity processors will deliver some improvement, exploiting parallelism through a variety of processor technologies using scalar, vector, multithreading and* **hardware accelerators** *(e.g.,* **FPGAs** *or ClearSpeed co-processors) creates the* ***greatest opportunity*** *for application acceleration."* => ***Cray XT5h***

+ HP, SRC, Nallatech, DRC, XtremeData, Inc. .....

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Contents

- **Background: Why FPGAs?**
- **ORNL success: FPGA systems, tools and up to 100x speedup**
- **Partners:** XILINX® **Research Lab,** UT**, SRC**
  mitrion CRAY sgi

OAK RIDGE National Laboratory

Future Supercomputer Technologies

Future Supercomputer Technologies

Commodity: **2^n** *multi* **=>** *many core*

Special: *El Dorado, Cyclops, PiM*

Future Supercomputer Technologies

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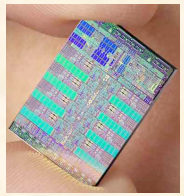
Accelerators



ClearSpeed

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Future Supercomputer Technologies

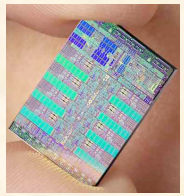
Commodity: 2^n *multi* => *many core*

Special: *El Dorado, Cyclops, PiM*

Accelerators

- **FPGA**: DSP => HPEC => HPC <==

- **Cell**: IBM, Sony, Toshiba



- **GPUs**: on *μ*P?

- **Array**: ClearSpeed

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What's an FPGA? Your "custom chip"

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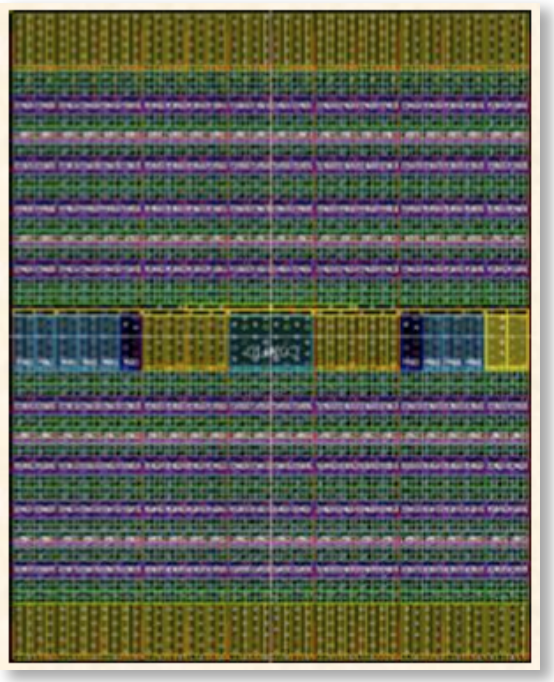
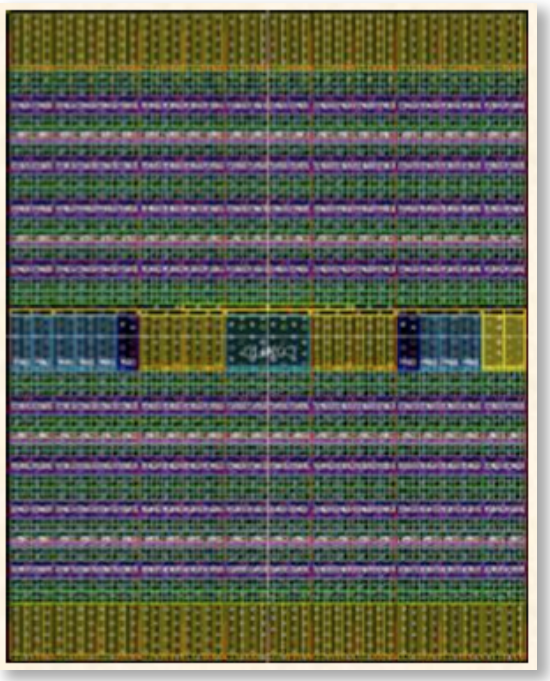
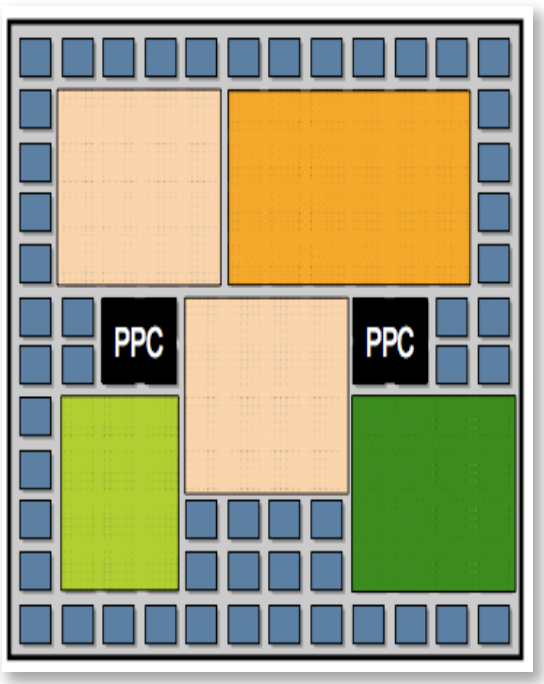


Xilinx Virtex4 FPGA:

What's an FPGA? Your "custom chip"





Xilinx Virtex4 FPGA: 89K slices (miniCPUs)

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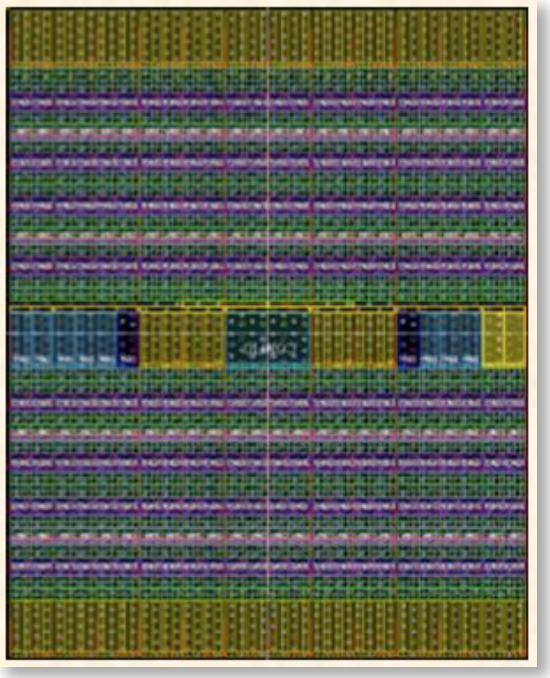

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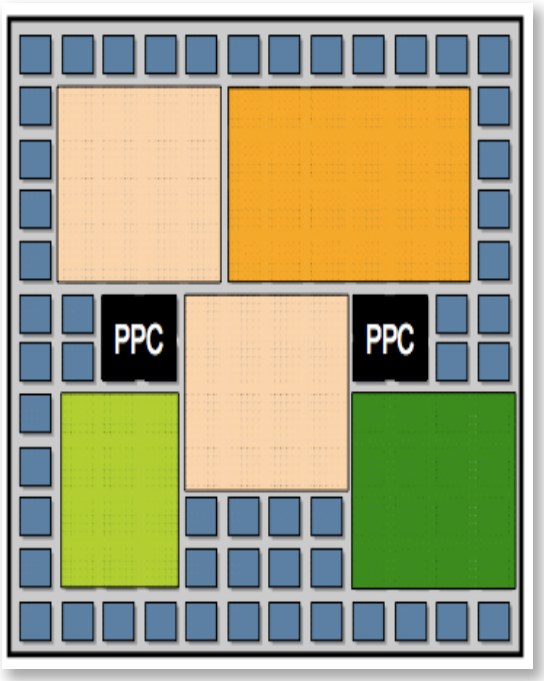

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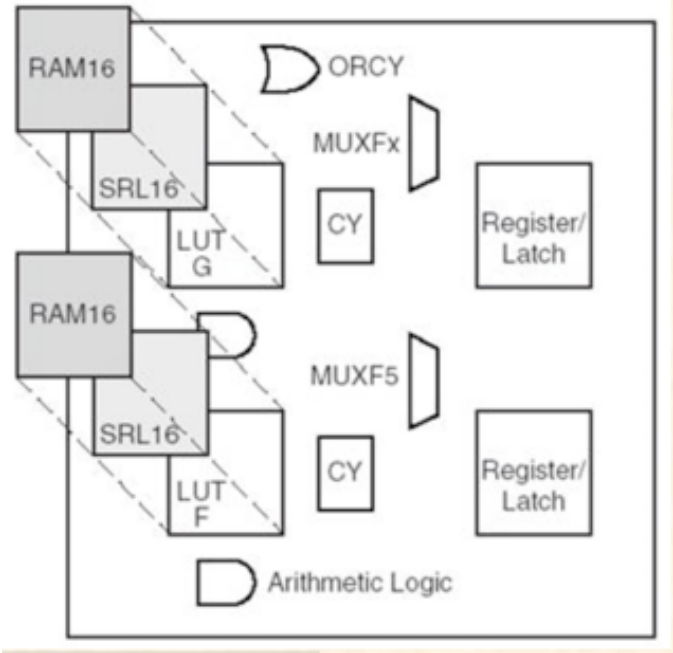

FPGA Logic slice

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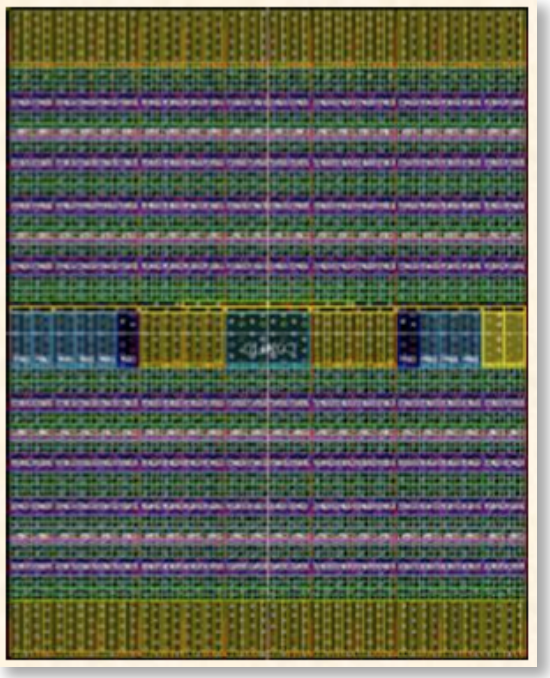

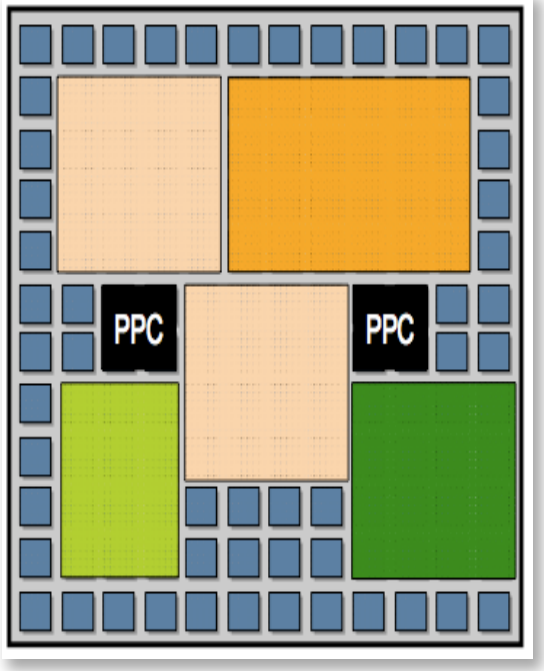

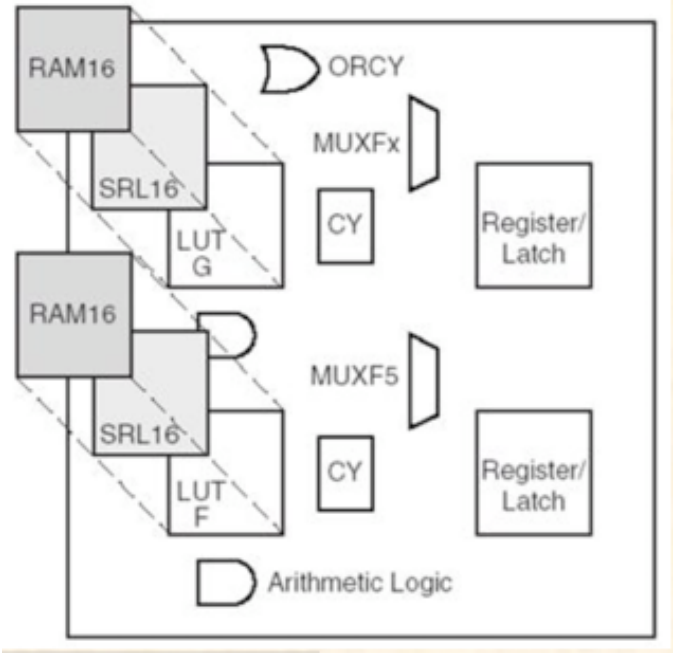

Xilinx Virtex4 FPGA: 89K slices (miniCPUs) FPGA Logic slice

- Logic array: user-tailored to application
- On-chip RAM, multipliers & PowerPCs
- Gigabit transceivers/DSP blocks => FastIO/precision
- 100–1000 operations/clock cycle

Why FPGAs?

Why FPGAs?

- **Performance**: optimal silicon use (maximize parallel ops/cycle)
- **Rapid growth**: Cells, Speed, I/O
- **Power**: 1/10th CPUs
- **Flexible**: *tailor* to application
- **Advances**: Telecom industry spinoff

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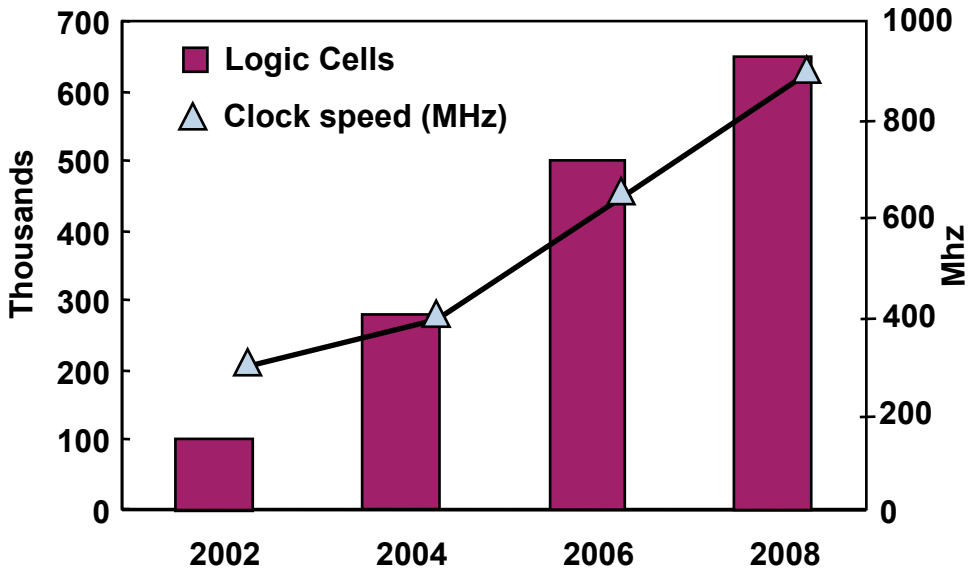

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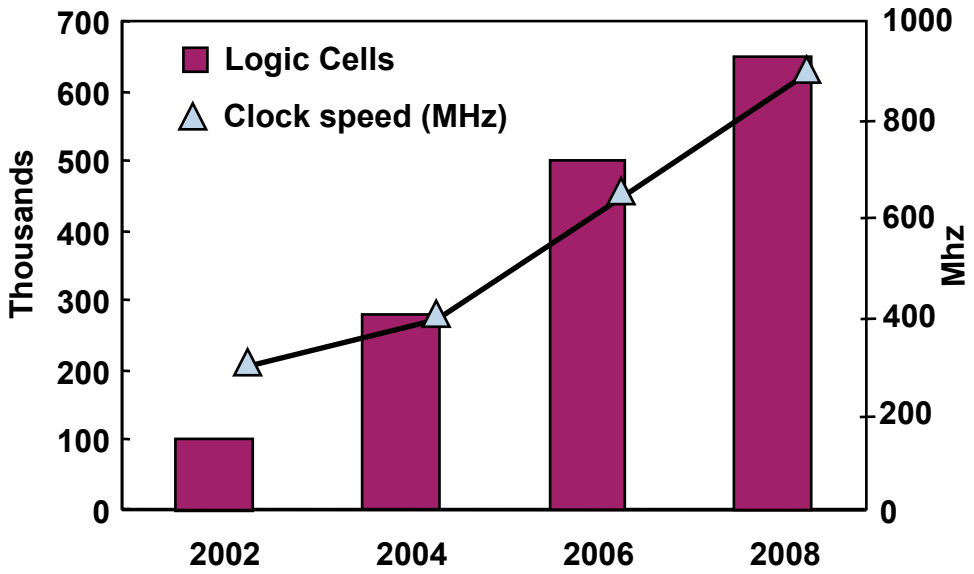
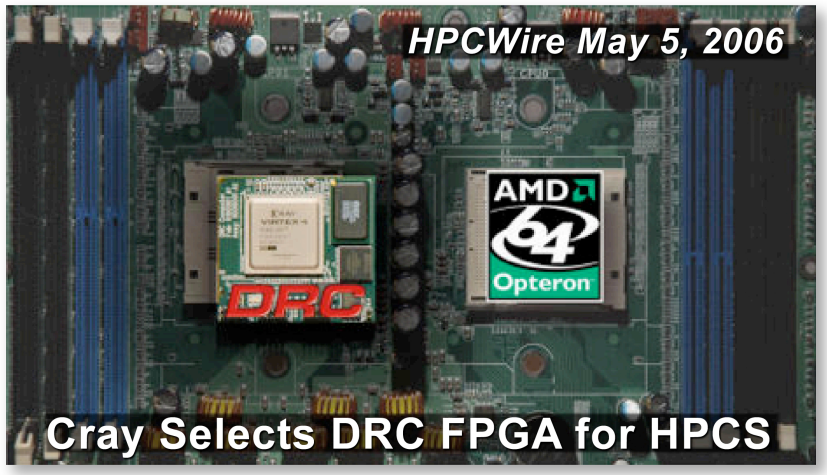
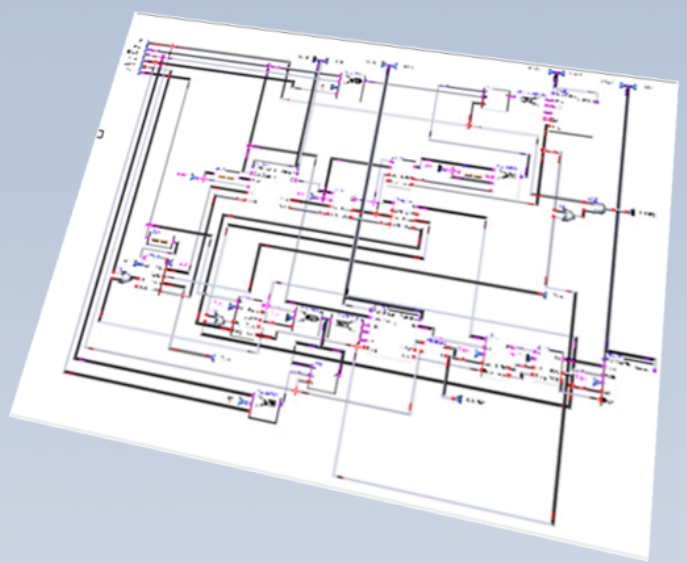




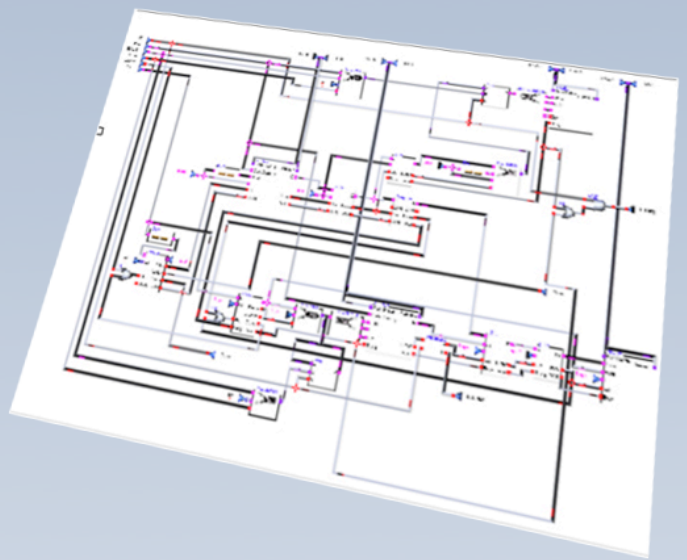
Exploring programming options



Viva: Graphical Icons—3-dimensional

Exploring programming options

Gauss matrix solver



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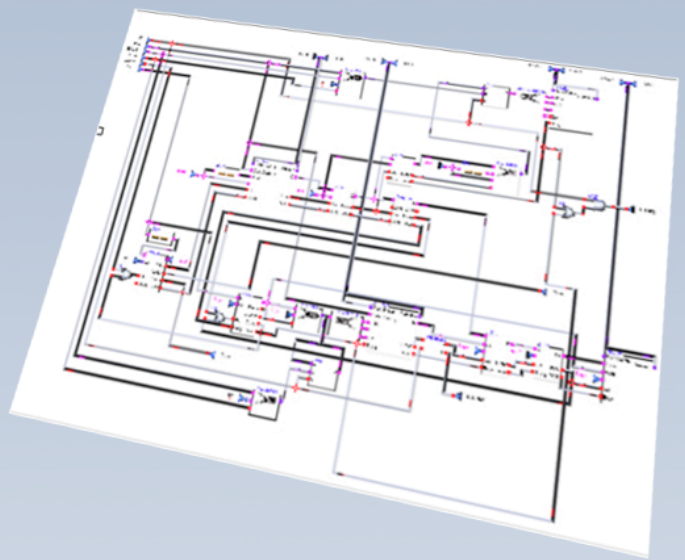

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Compiler, simulator, and debugger

MitrionC: Text/flow—1-dimensional

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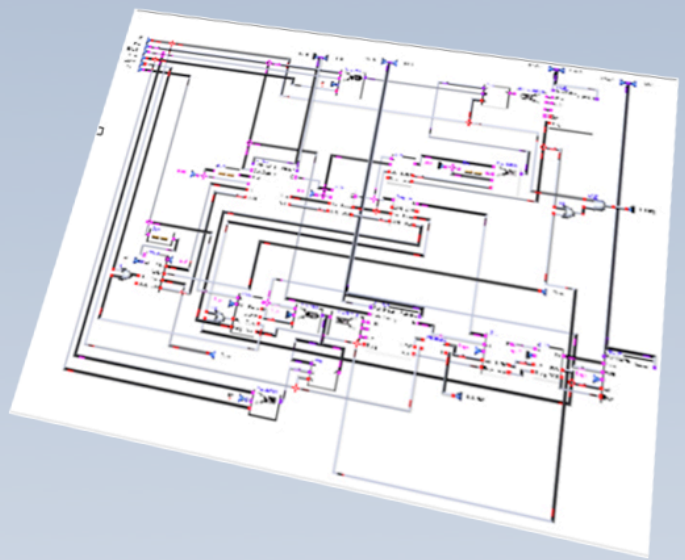


Viva: Graphical Icons—3-dimensional

Compiler, simulator, and debugger

MitrionC: Text/flow—1-dimensional

+ Carte/SRC, CHiMPS-VHDL/Xilinx , DSPlogic

Applications

Applications

- Genomics
- Matrix Equation Solution
- Molecular Dynamics, Weather/Climate

Openfpga.org Smith-Waterman Benchmark

- ***FASTA*** ***(University of Virginia) application***

  http://fasta.bioch.virginia.edu

- **Uses search34 code & Cray SWA core**

- **Human Genome Data: 4GB compressed**

  3685 searches (MPI on ORNL Cray XD1)

Alignment of ACGAACCCTTGC and ACGTATGC

	0	A	C	G	T	A	T	G	C
0	0	0	0	0	0	0	0	0	0
A	0	2	0	0	0	2	0	0	0
C	0	0	4	2	1	0	1	0	2
G	0	0	2	6	4	3	2	3	1
A	0	2	1	4	5	6	4	3	2
A	0	2	1	3	3	7	5	4	3
C	0	2	4	2	2	5	6	4	6
C	0	0	2	3	1	4	4	5	6
C	0	0	2	1	2	3	3	3	7
T	0	0	0	1	3	2	5	3	5
T	0	0	0	0	3	2	4	4	4
G	0	0	0	2	1	2	2	6	4
C	0	0	2	0	1	0	1	4	8

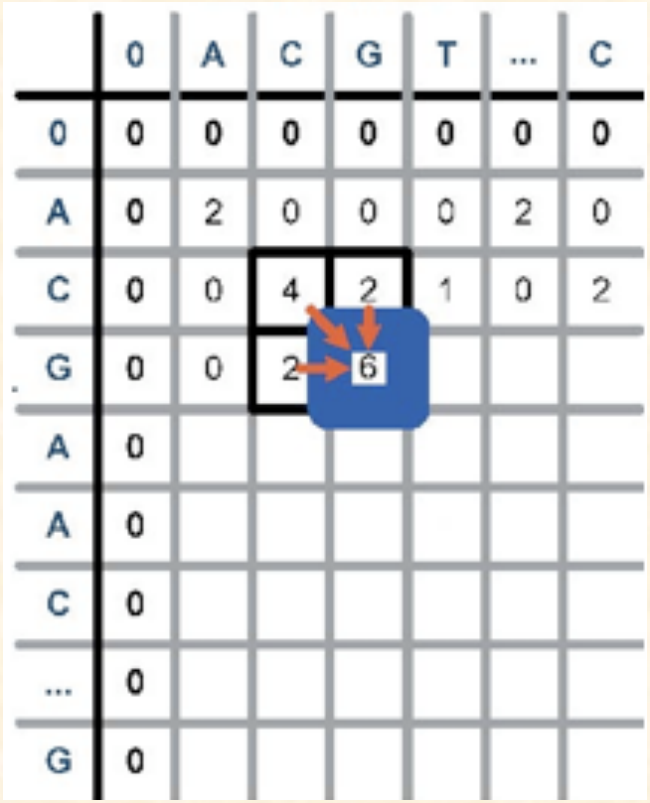
Final alignment

A	C	G	A	A	C	C	C	T	T	G	C
	|	|		|					|	|	|
A	C	G	T	A	-	-	-	-	T	G	C

Smith-Waterman Algorithm Scoring

Query Sequence

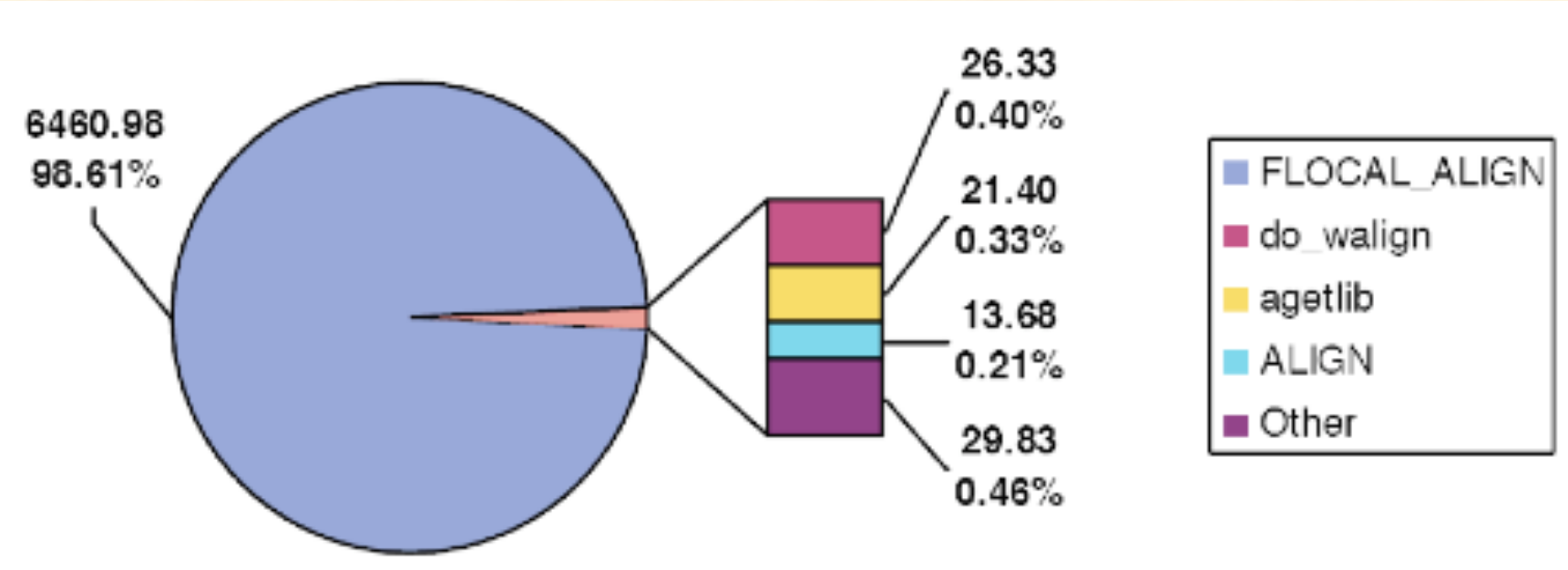
Database Sequence



	0	A	C	G	T	...	C
0	0	0	0	0	0	0	0
A	0	2	0	0	0	2	0
C	0	0	4	2	1	0	2
G	0	0	2	6			
A	0						
A	0						
C	0						
...	0						
G	0						

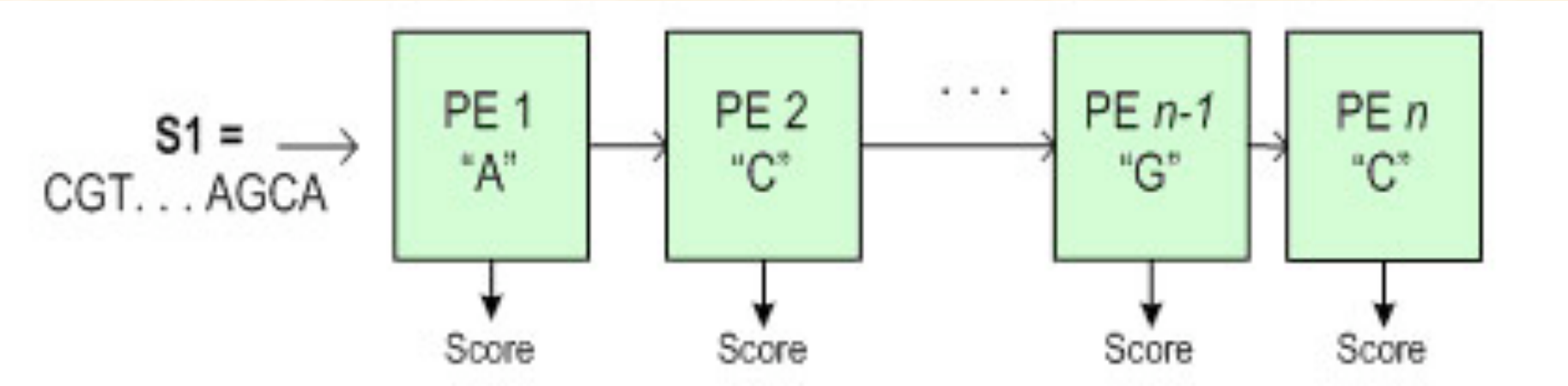
1. Initialize row & column 1 to 0
2. Score matches from upper left
3. Add to above-left score *(2+4=6)*

Search34 Computation Profile



98.61% is FLOCAL_ALIGN => VHDL kernel

Smith-Waterman Pipeline



1. Query character preloaded into each PE
2. String S1 shifted thru pipe to compare
3. Score generated

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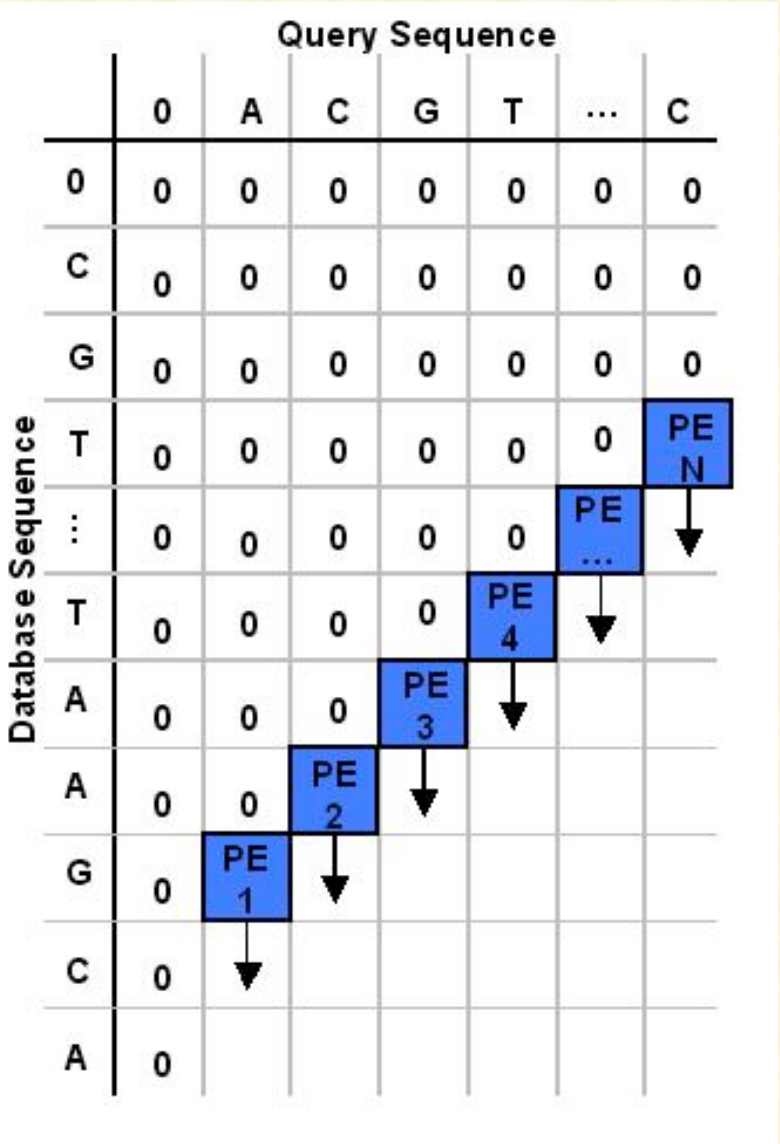
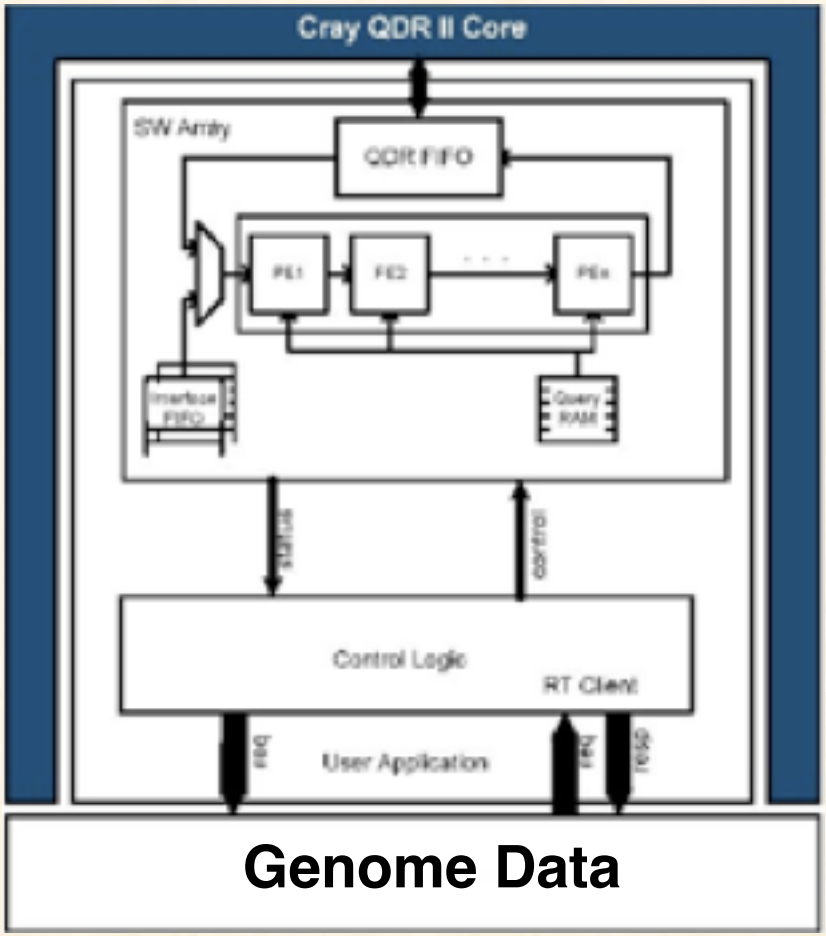
Smith-Waterman

Parallel Score Calculation



Overall Algorithm



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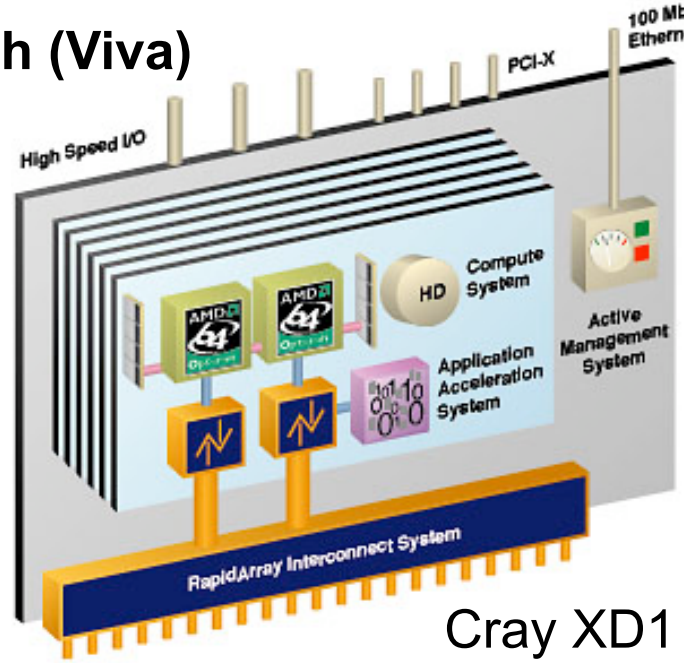
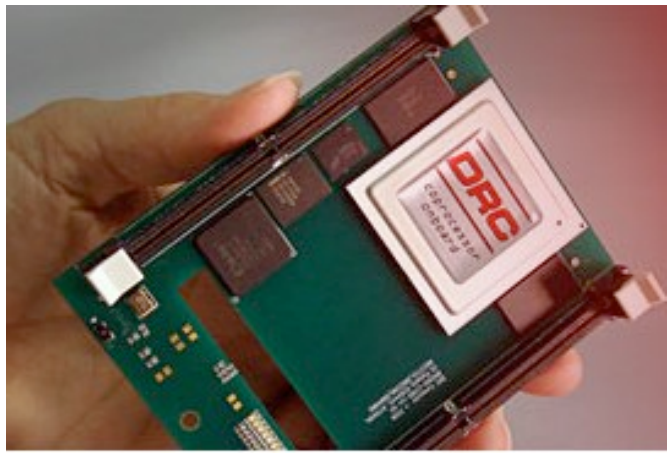
IBM Cell BladeCenter

ORNL FPGA hardware/tools

- SRC-6 (Carte), Digilent (Viva, VHDL), Nallatech (Viva)
- Cray XD1 (MitrionC, VHDL):
  6 FPGAs + 144 Opterons
- SGI RASC-Altix/Virtex4s (MitrionC)
- CHiMPS (Bee2 => Cray XD1 => DRC => XT4)
  (Xilinx early access)



Cray XD1



FPGA Performance

ORNL XD1 (Virtex2): Initial Results

Case 1: *Micro-RNA*

FPGA Performance

ORNL XD1 (Virtex2): Initial Results

Case 1: *Micro-RNA*

FPGA vs Opteron Time (hrs) for FASTA

	1	2	3	4	5
CPU 2.2GHz	75	-	-	-	-
FPGA(s) 0.2GHz	7.39	3.75	2.48	1.91	1.56
FPGA Speedup vs 1 CPU	10.15	20.0	30.2	39.3	48.1

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Output Options (Impact Speedup)

Detailed: -Q -H -f -10 -g -3 -d 10 -b 10 -s OpenFPGA.mat -E 0.0001
Minimal: -Q -H -f -10 -g -3 -d 0 -b 10 -s OpenFPGA.mat -E 0.0001

Cray XD1 FPGA Speedup vs. 2.2 GHz Opteron
Case 2: *Bacillus anthracis DNA comparison*

8k

16k

8k

16k

Cray XD1 FPGA Speedup vs. 2.2 GHz Opteron

Case 2: *Bacillus anthracis DNA comparison*

Virtex2 Pro 50 Speedup

	24	*25*	*26*	*27*	*28*	*29*	*30*	*31*	*32*	*33*	*34*	*35*	*36*	*37*	*38*	*39*	*40*	*41*	*Avg*	*SD*
8k	26	30	27	32	30	30	29	30	30	27	31	29	31	30	31	31	31	30	29.6	1.2
16k	22	25	26	31	30	30	28	31	28	27	30	29	29	29	32	31	32	29	28.7	2.5
8k	49	49	49	50	49	49	50	49	49	49	49	49	49	49	50	49	49	49	49.4	0.2
16k	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	49	50	50	49.9	0.3

24 => Sequence AE017024

Cray XD1 FPGA Speedup vs. 2.2 GHz Opteron

Case 2: *Bacillus anthracis DNA comparison*

Virtex2 Pro 50 Speedup

	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	Avg	SD
8k	26	30	27	32	30	30	29	30	30	27	31	29	31	30	31	31	31	30	29.6	1.2
16k	22	25	26	31	30	30	28	31	28	27	30	29	29	29	32	31	32	29	28.7	2.5
8k	49	49	49	50	49	49	50	49	49	49	49	49	49	49	50	49	49	49	49.4	0.2
16k	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	49	50	50	49.9	0.3

Virtex4 LX160 Speedup: 8 hrs => 5 mins*

	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	Avg	SD
8k	36	43	39	47	44	45	43	45	45	39	46	42	46	44	46	46	46	43	43.5	2.9
16k	29	33	37	45	44	43	39	47	41	37	46	41	43	41	47	46	48	43	41.5	4.9
8k	98	98	98	97	97	98	98	98	98	97	98	98	98	98	98	98	98	97	97.6	0.1
16k	100	101	101	100	100	100	101	101	101	101	101	101	101	101	100	100	101	100	100.7	0.4

*28,873 => 288 secs

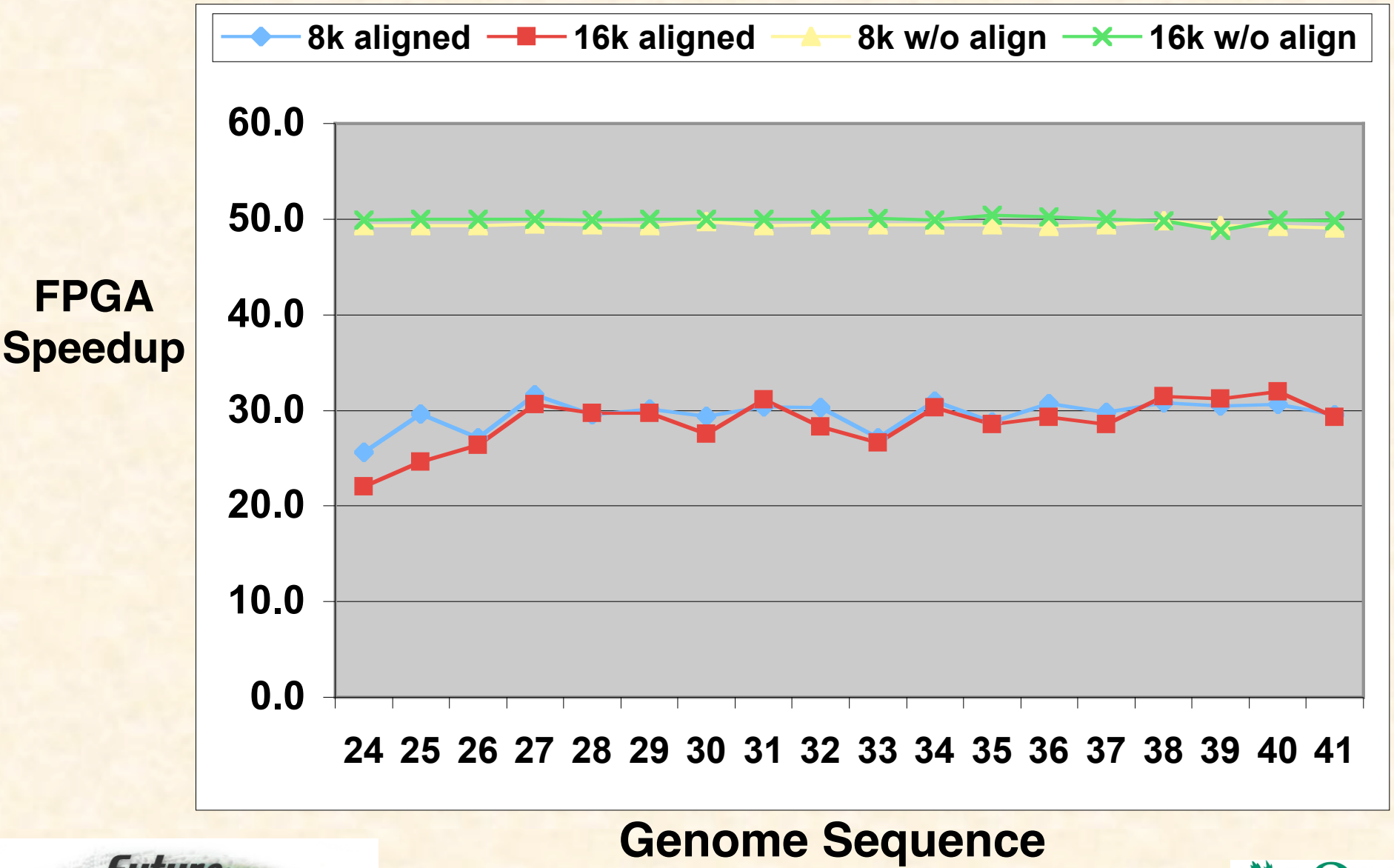
24 => Sequence AE017024

XD1 Virtex2 Speedup vs. 2.2 GHz Opteron

Case 2: *Bacillus anthracis DNA comparison*

XD1 Virtex2 Speedup vs. 2.2 GHz Opteron

Case 2: *Bacillus anthracis DNA comparison*



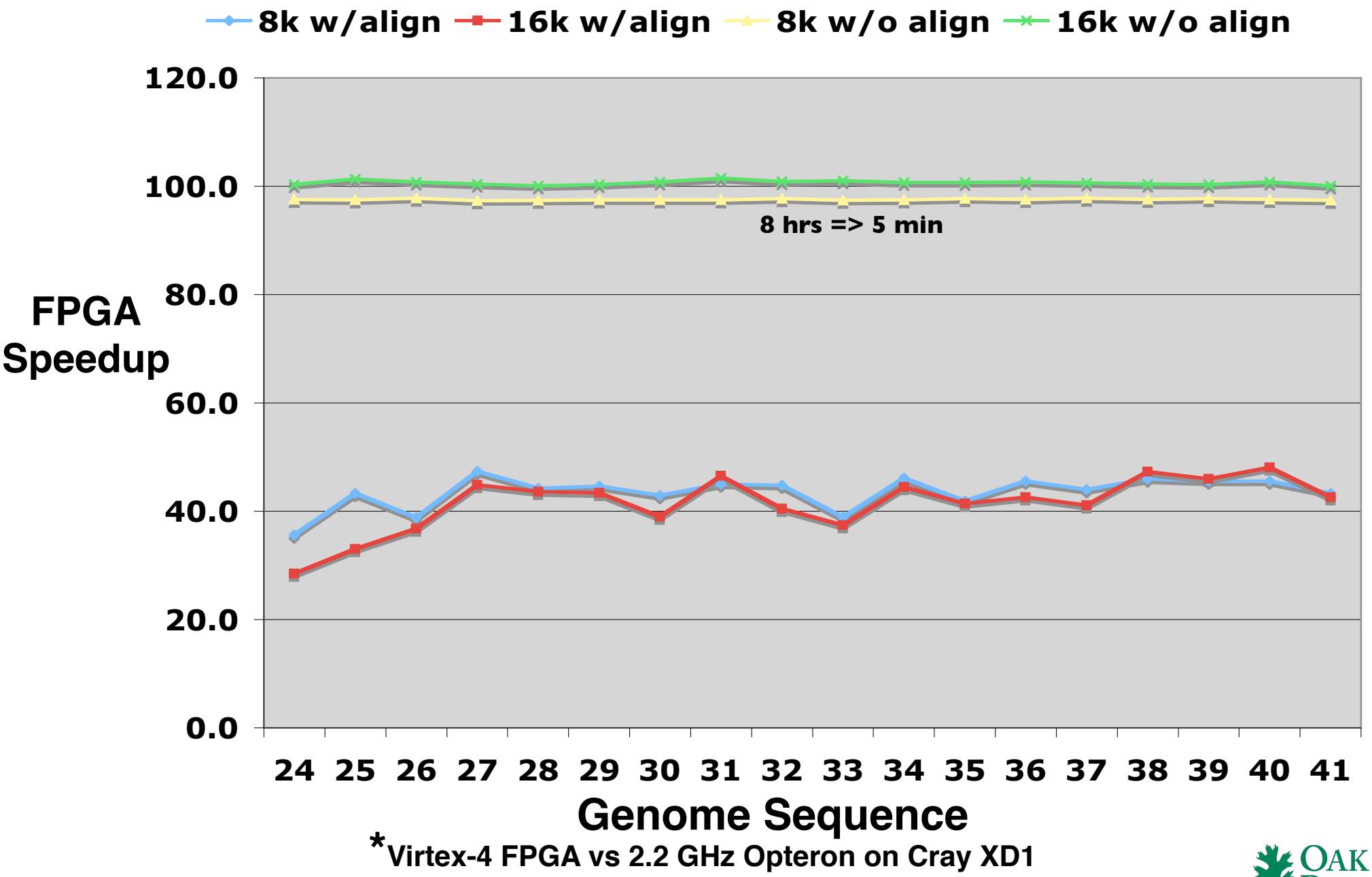
100x* DNA Sequence Speedup

Bacillus anthracis Human DNA comparison

*Virtex-4 FPGA vs 2.2 GHz Opteron on Cray XD1

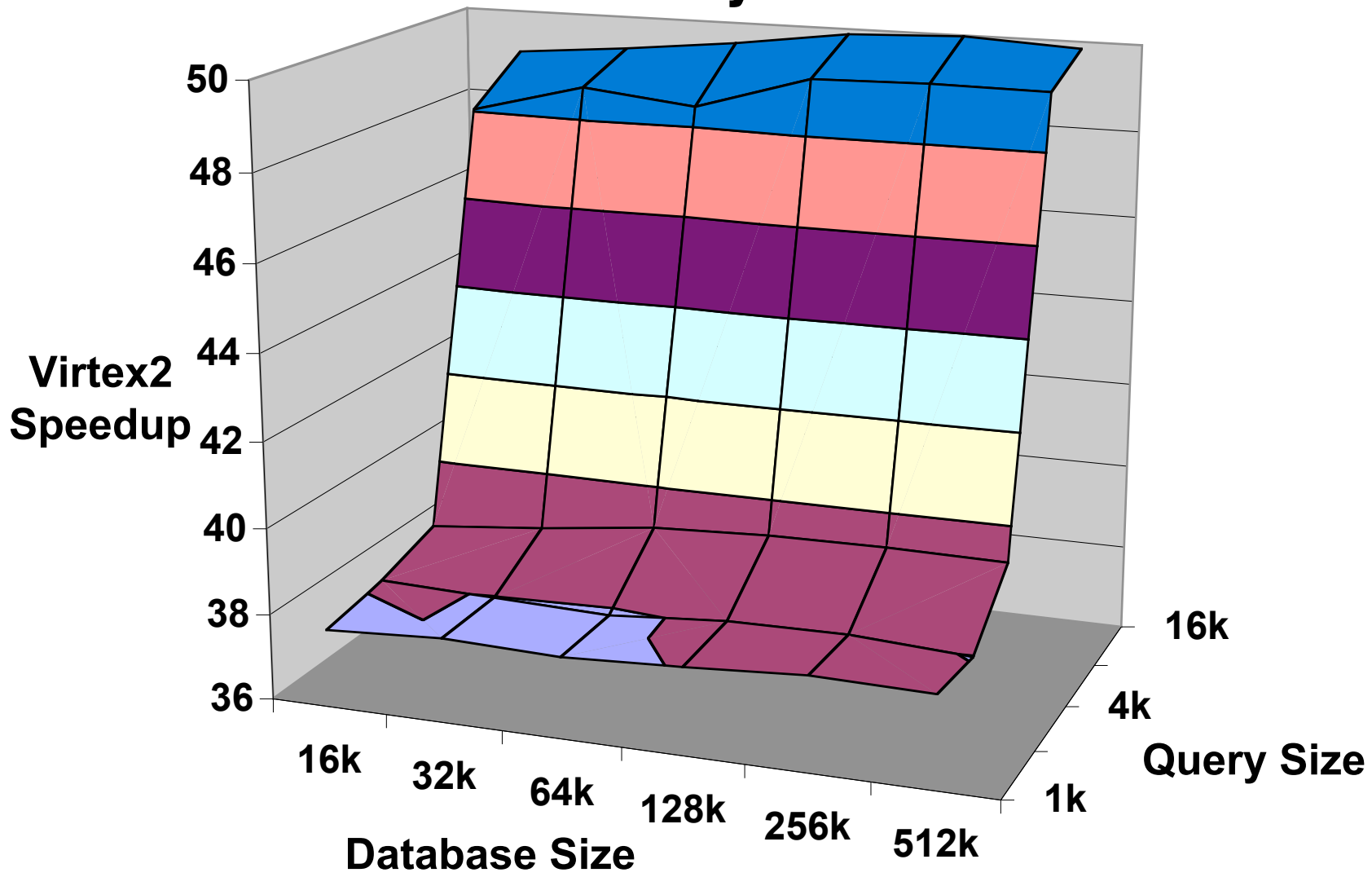
100x* DNA Sequence Speedup

Bacillus anthracis Human DNA comparison



*Virtex-4 FPGA vs 2.2 GHz Opteron on Cray XD1

FPGA Speedup Grows with Query Size



Preliminary Results: 150 FPGAs*

*Thanks to NRL for use of 150 FPGA Cray XD1

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Solve large DNA sequencing problem:
12.5 years (150 mos.) for 1 Opteron

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Preliminary Results: 150 FPGAs*

Solve large DNA sequencing problem:
12.5 years (150 mos.) for 1 Opteron

6 weeks for 150 Opterons

*Thanks to NRL for use of 150 FPGA Cray XD1

Preliminary Results: 150 FPGAs*

Solve large DNA sequencing problem:

12.5 years (150 mos.) for 1 Opteron

6 weeks for 150 Opterons

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Next: Test performance on *64 Virtex4 FPGA Maxwell* at Edinburgh University

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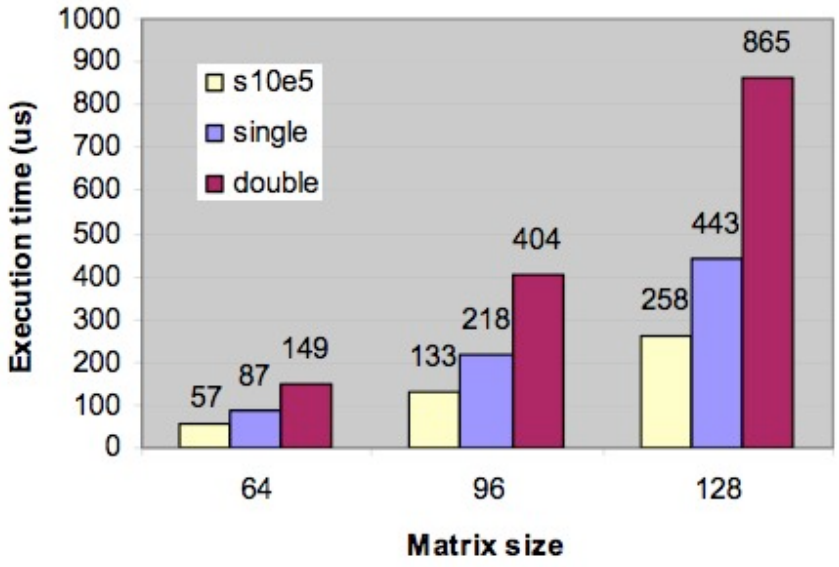
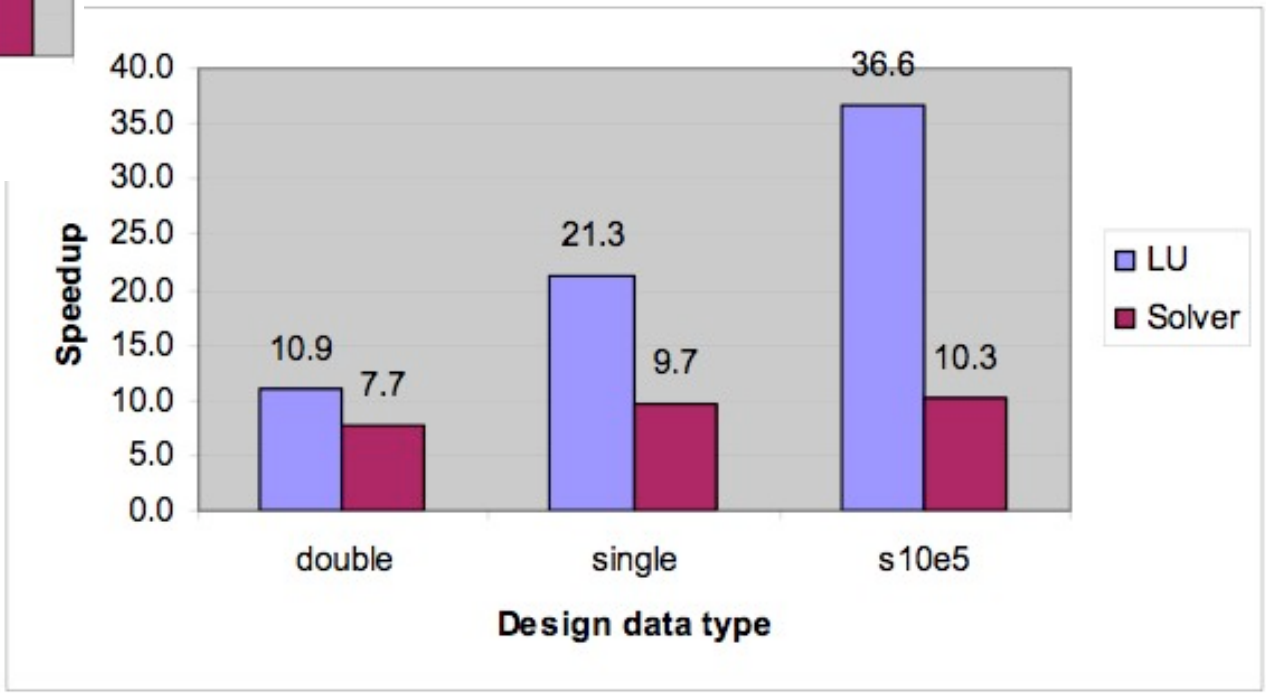
37x* LU Decomposition FPGA Speedup
10x for Matrix Equation Solver





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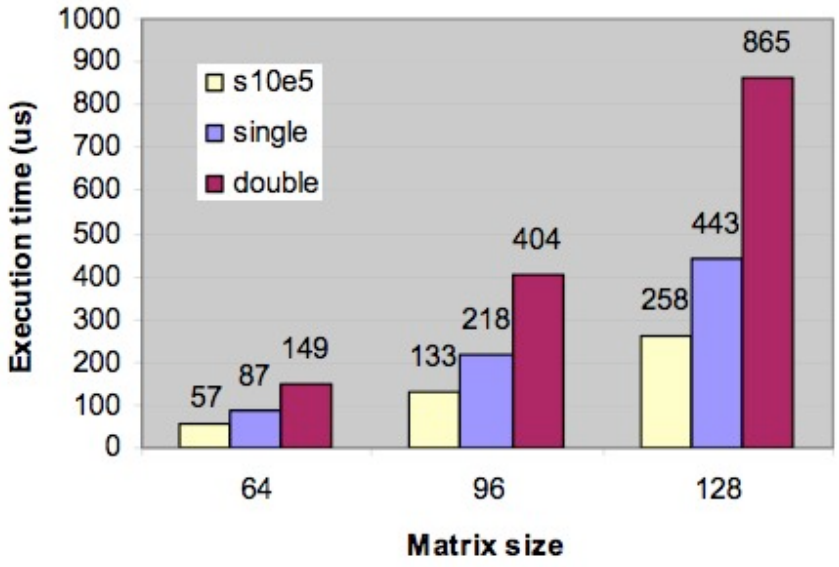

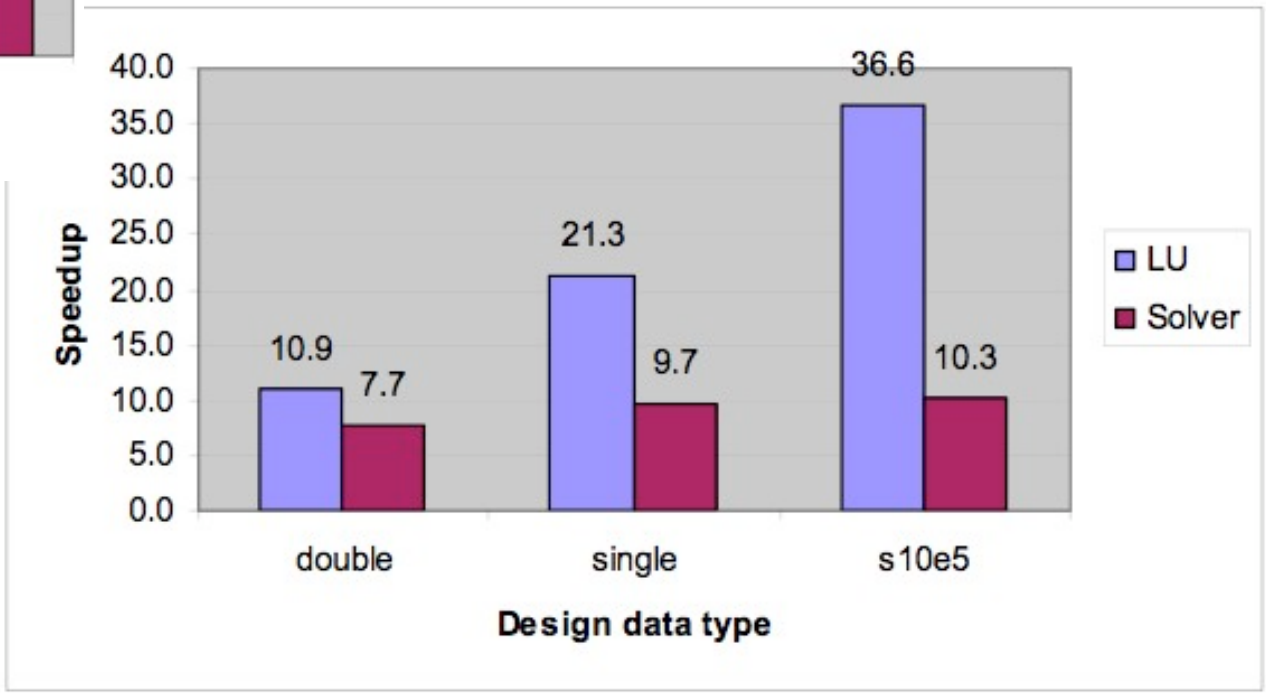

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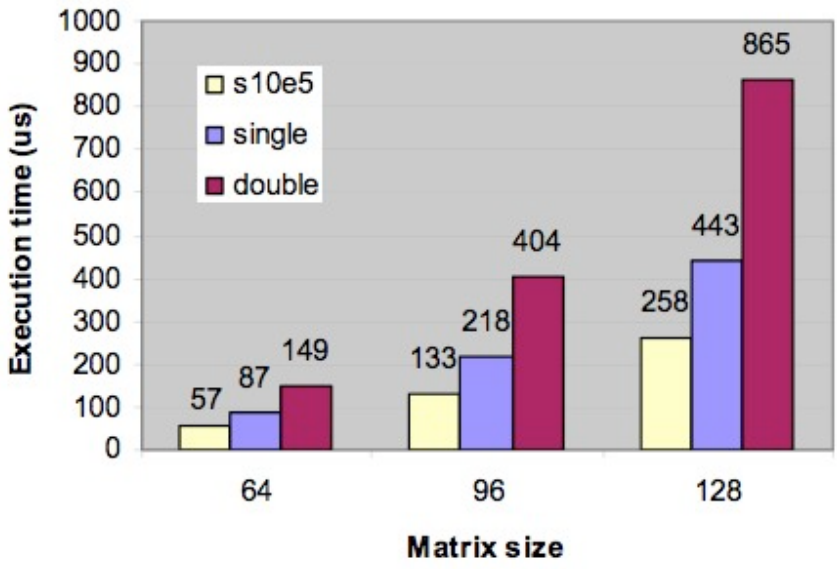

Table 6: LU implementation on XC2VP50-7

Design	Double FP	Single FP	S10e5
PE amount	8	16	32
Max size	128	256	256
Achievable Frequency	120MHz	150MHz	150MHz
Slices	27,005 (57%)	14792 (59%)	14730 (62%)
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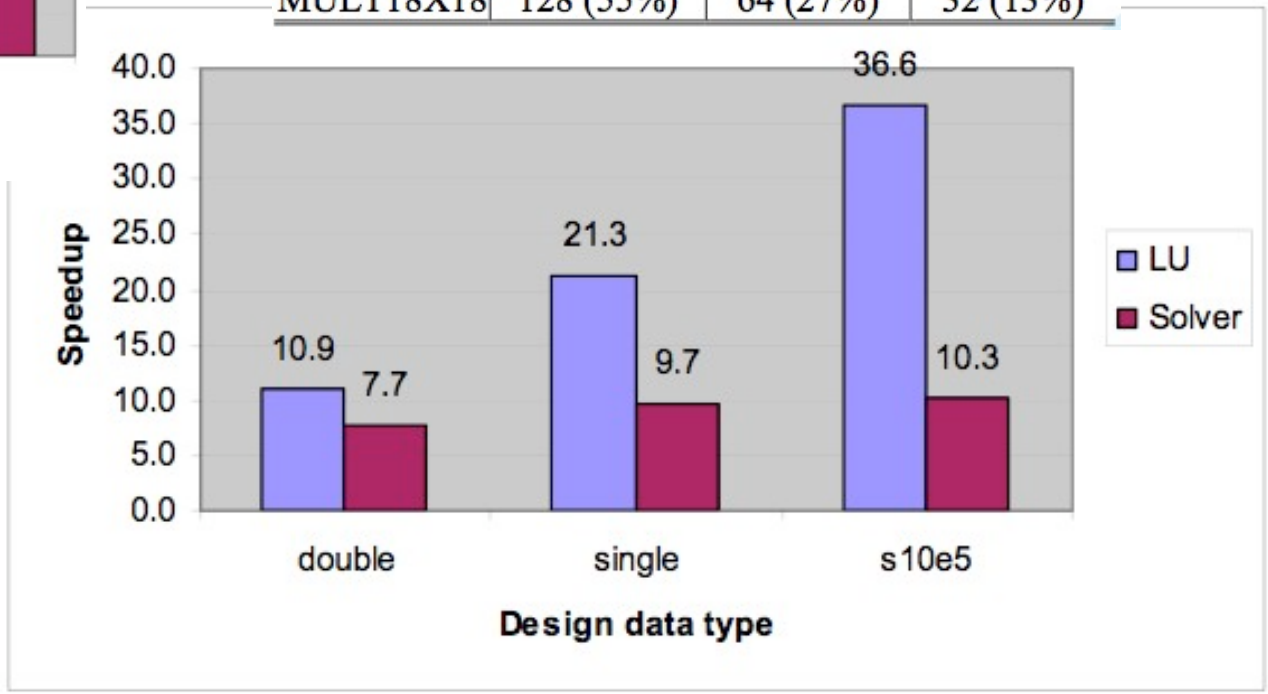

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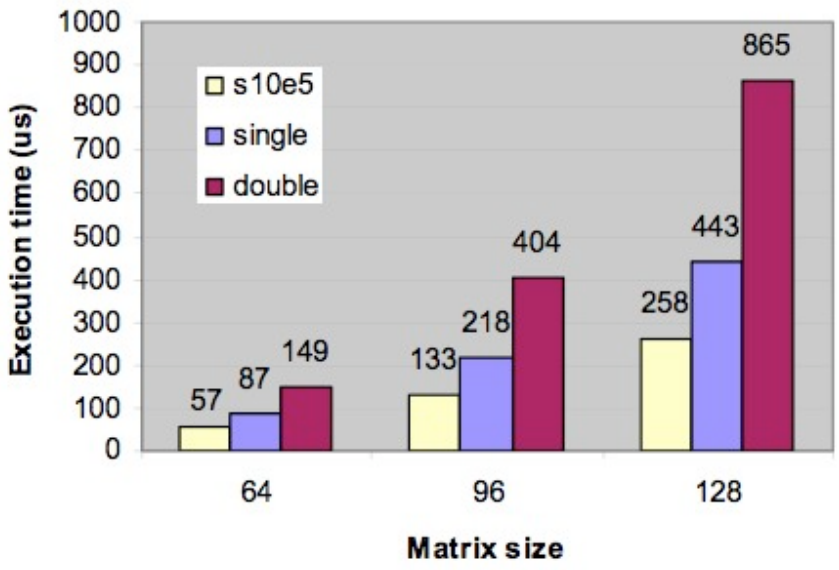

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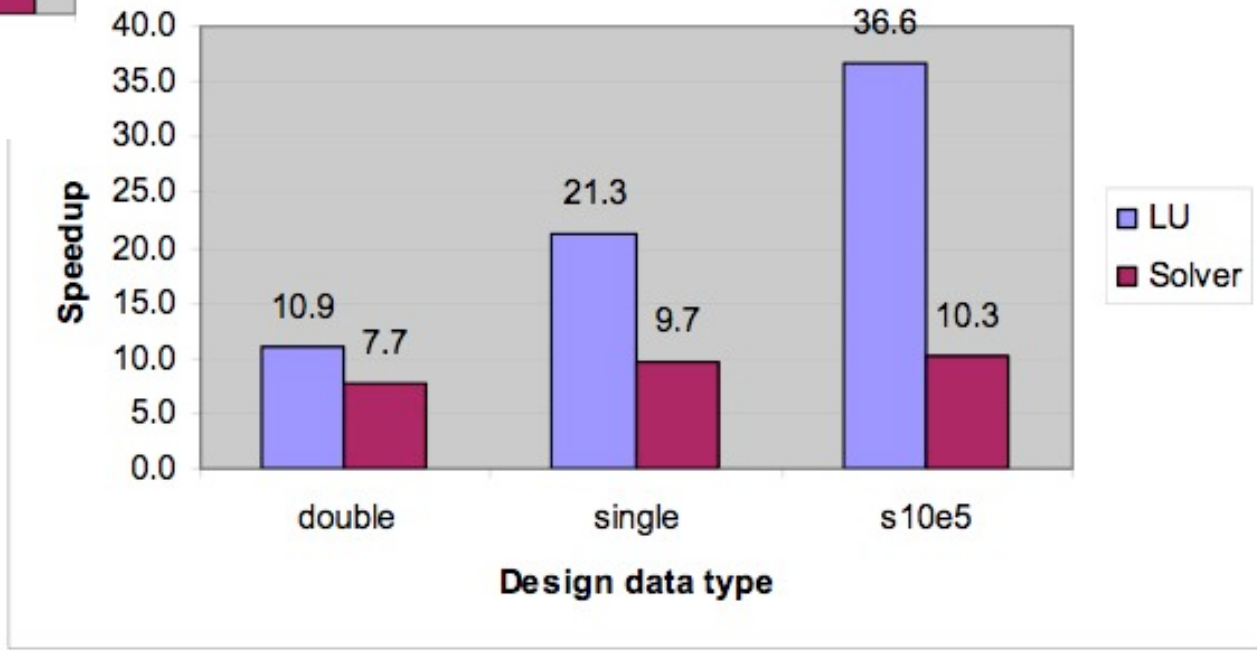

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High performance **of LP arithmetic**

High precision **accuracy**

Speedup increases **with matrix size**
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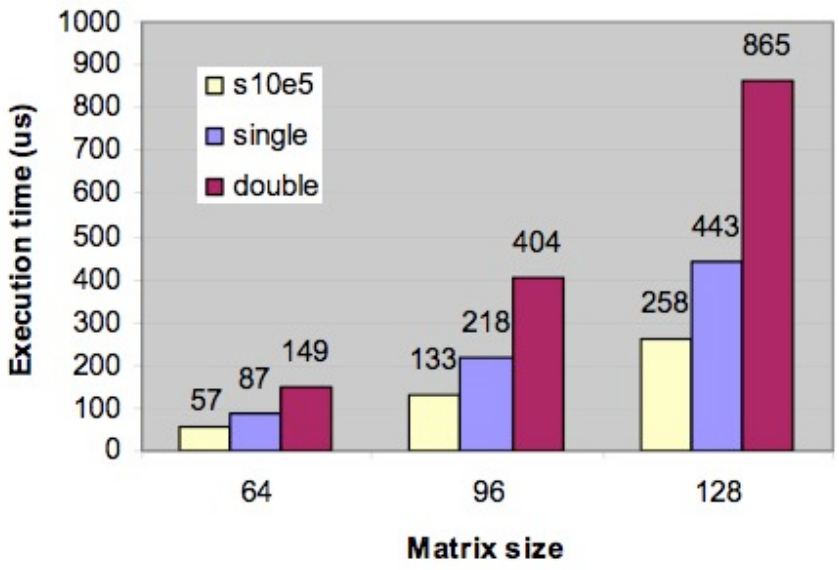

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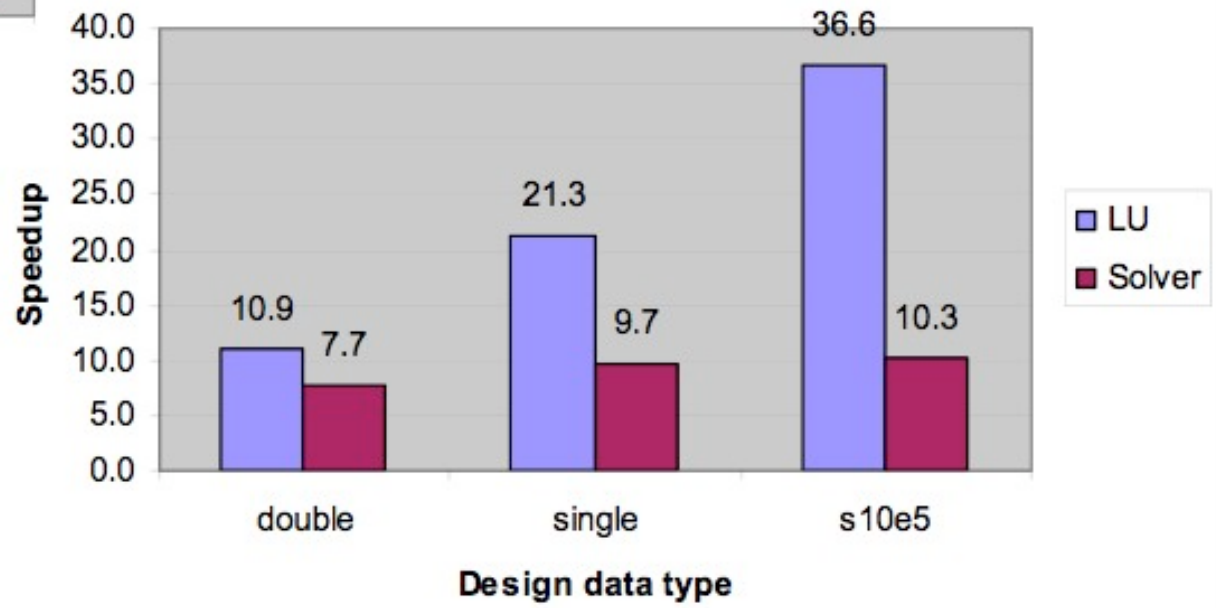

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First mixed-precision LU & solver for FPGAs

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Ported Weather-Climate code Spectral Transform Shallow Water Model (STSWM) to FPGAs

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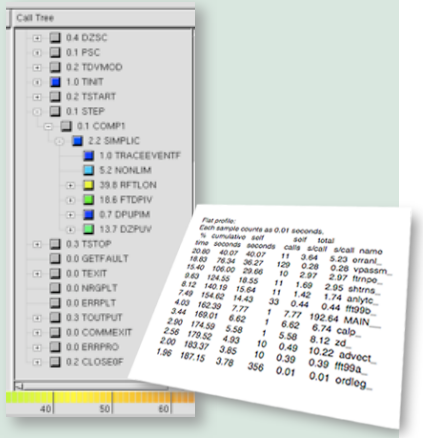
Profile



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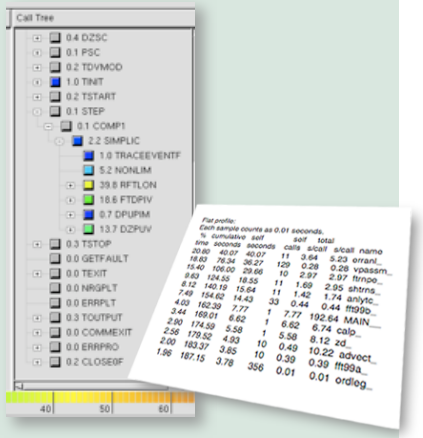
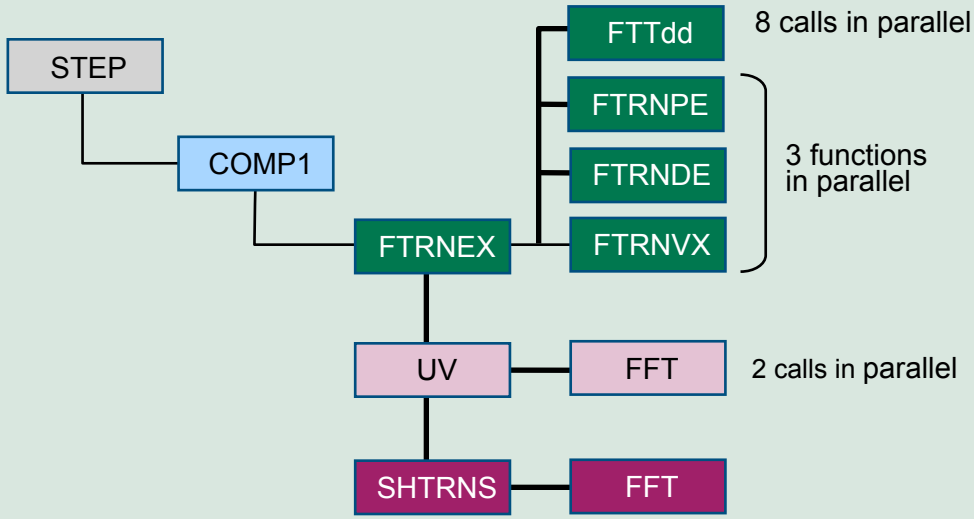


Find parallelism: 80% FFTs



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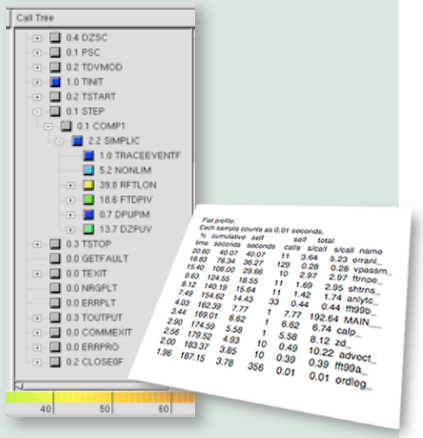

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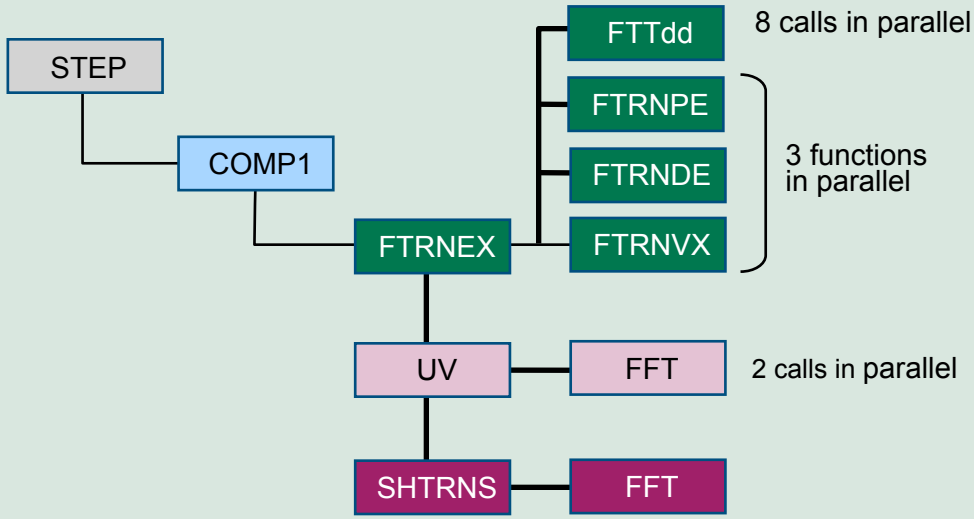
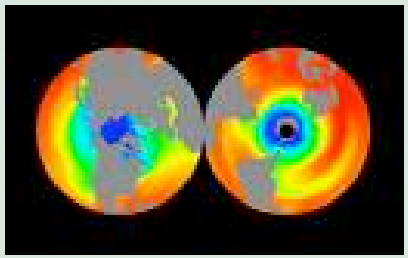


Goal

More GF/$ GF/Watt



Model 5-10X faster

Summary

- ORNL FPGA research:

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Contact

Olaf O. Storaasli
Future Technologies Group
Google **Olaf ORNL**

THANK YOU

OAK RIDGE National Laboratory

Context

ORNL Jaguar Supercomputer Advances to Second in the World

System is the world's most powerful for open science

102TF 2Q07 => 250TF 4Q07 => 1PF 4Q08

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