ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

CSCS
Swiss National Supercomputing Centre

Towards a hybrid multi-core implementation of MAQUIS Exact Diagonalization (ED)

Sergei Isakov, Will Sawyer, Adrian Tineo, Gilles Fourestey, Neil Stringfellow, Matthias Troyer

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  - MPI + OpenMP hybrid programming
  - MPI-2 one-sided communication
  - SHMEM
  - UPC (as implemented in Cray compiler)
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- Compare performance across platforms
  - out-of-the-box performance
  - evaluate optimization effort
  - socket-for-socket, node-for-node comparisons

CSCS Testbed Platforms

System name	Rivera	Sandy	Castor
Processor	AMD 6274	Intel E5-2680	Intel X5650
Proc. nickname	Interlagos	Sandybridge	Westmere
Clock (GHz)	2.2	2.7	2.66
Sockets/Node	2	2	2
Cores/Socket	16	8	6
NUMA/Socket	2	1	1
DP GFlops/Socket	140.8	172.8	63.8
Memory/Socket	16 GB	16 GB	12 GB
DDR3 mem. speed	1600	1333	1333
L1 cache (excl.)	16KB	32KB	32KB
L2 cache/# cores	2MB/2	256KB/1	256KB/1
L3 cache/# cores	8MB/8	20MB/8	12MB/6
Hyperthreading?	no	yes (2)	unenabled
TPA/Socket (W)	115	130	95

Parallel Test Platforms

System name	Rosa	Todi	Rothorn	Grotius
Product name	Cray XE6	Cray XT6	SGI UV1000	IBM BG/Q
Interconnection	Gemini	Gemini	NUMAlink	5D Torus
Processor	AMD 6272	AMD 6272	Intel E7-8837	IBM A2
Proc. nickname	Interlagos	Interlagos	Westmere	
Clock (GHz)	2.1	2.1	2.66	1.60
Sockets/Node	2	1	32	1
Cores/Socket	16	16	8	16
NUMA/Socket	2	2	1	1
DP GFlops/Socket	134.4	134.4	85.1	204.8
Memory/Socket	16 GB	16 GB	64 GB	16 GB
DDR3 mem. speed	1600	1600	1333	1333
L1 cache (excl.)	16KB	16KB	32KB	32KB
L2 cache/# cores	2MB/2	2MB/2	256KB/1	32MB/16
L3 cache/# cores	8MB/8	8MB/8	24MB/8	N/A
Hyperthreading?	no	no	no	yes (4)
TPA/Socket (W)	115	115	130	60

Fundamental ED problem

$$H = J \sum S_i^z S_j^z + \Gamma \sum S_i^x$$

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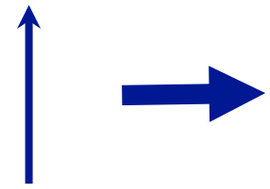

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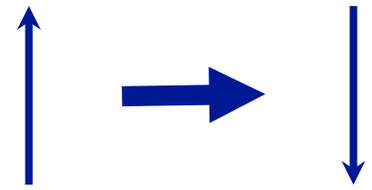

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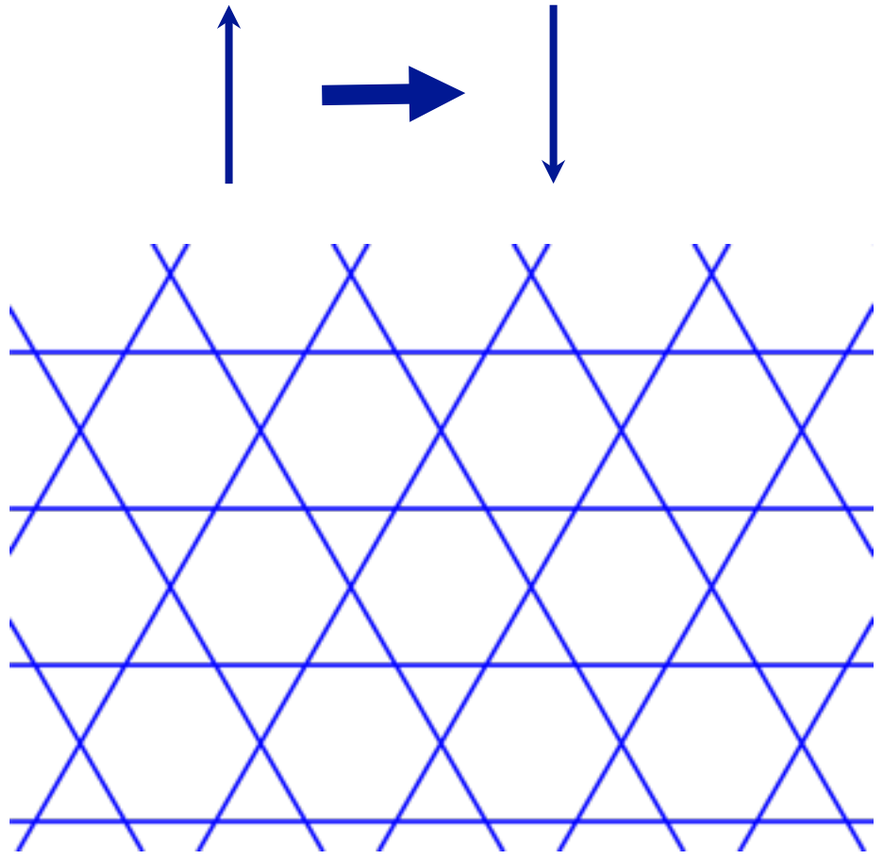

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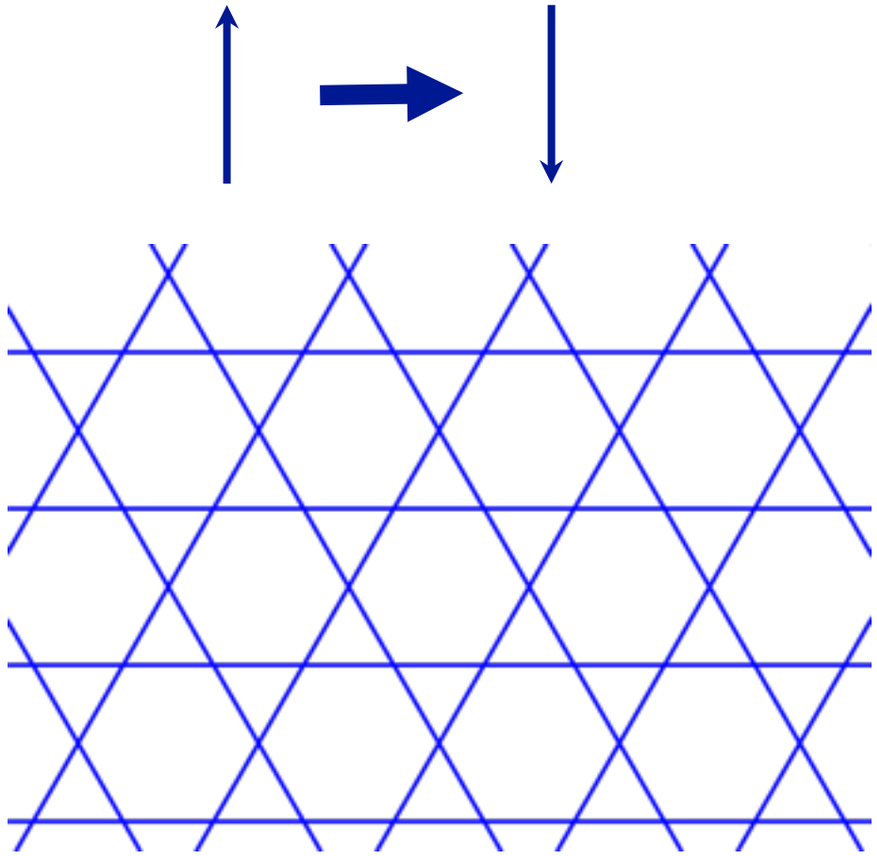

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1: $v_1 \leftarrow$ random vector with norm 1
2: $w_0 \leftarrow 0$
3: $\beta_1 \leftarrow 0$
4: **for** $j = 1, \ldots, r$ **do**
5: $\quad w_j \leftarrow Hv_j - \beta_j v_{j-1}$
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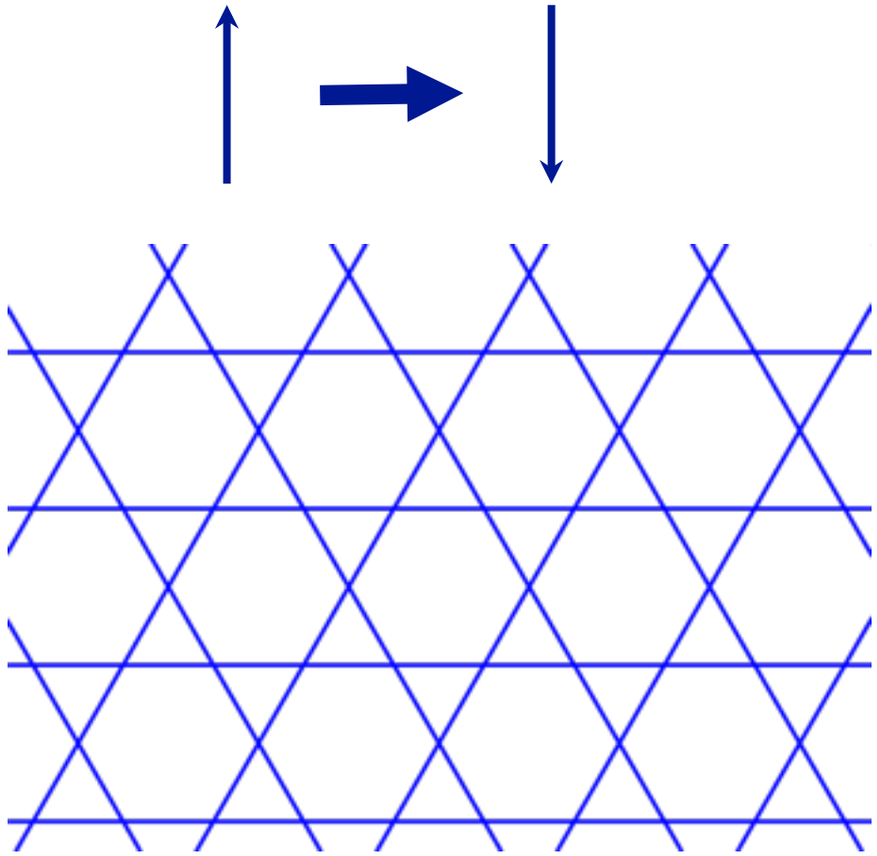

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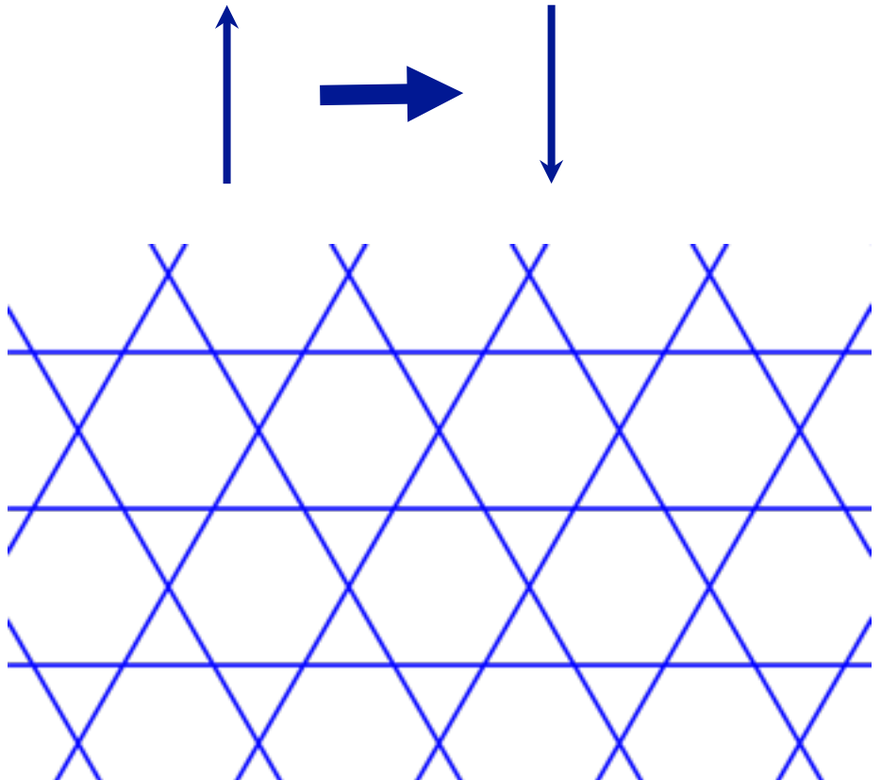

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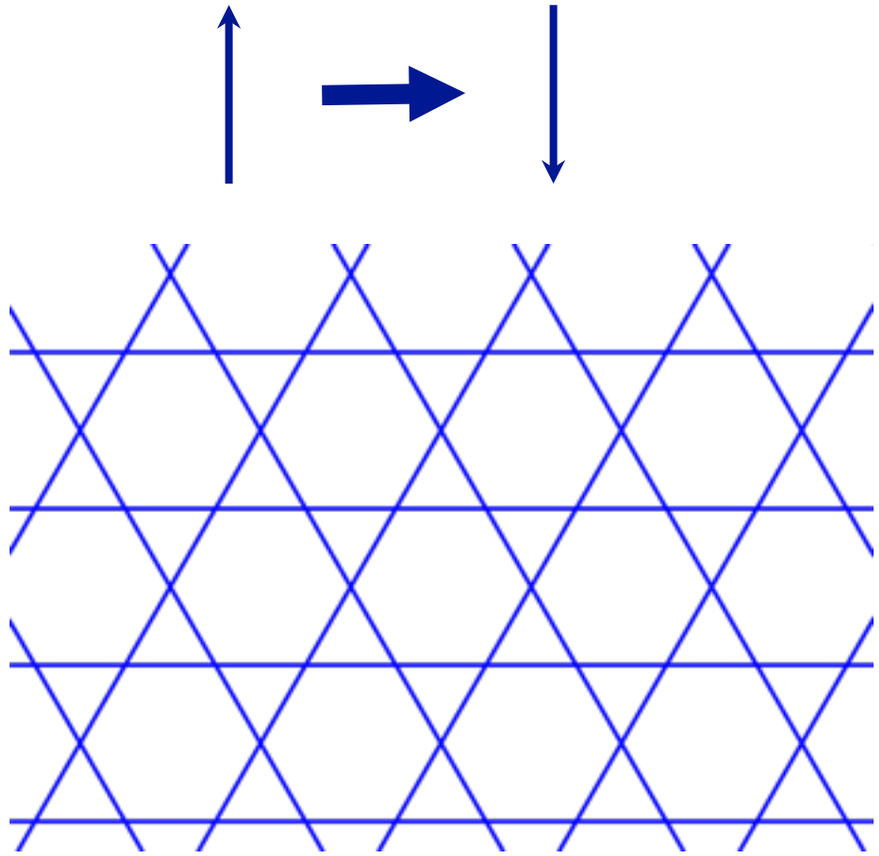

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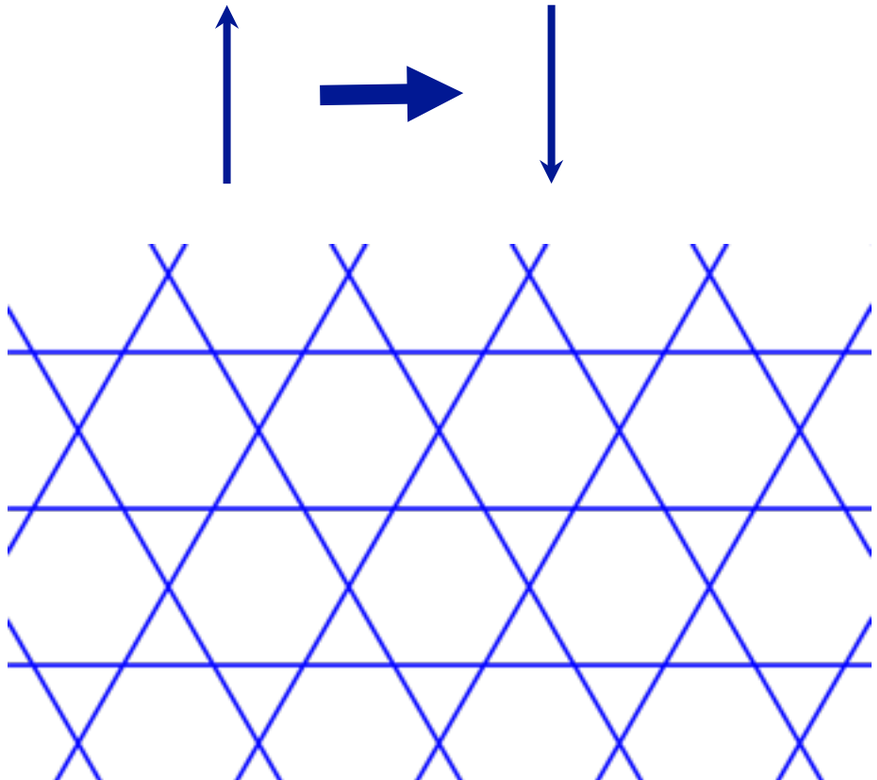
- Any lattice with n sites, 2^n states
- Lanczos eigensolver
- Large, sparse symmetric mat-vec



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- Any lattice with n sites, 2^n states
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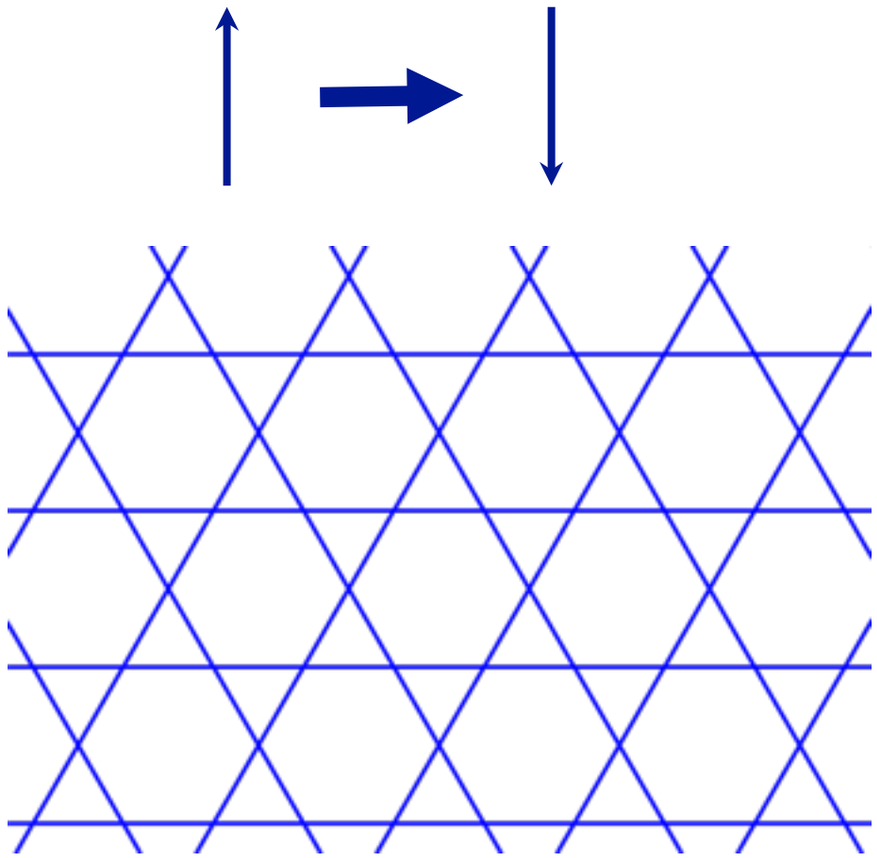
- Large, sparse symmetric mat-vec
- Operator has integer operations



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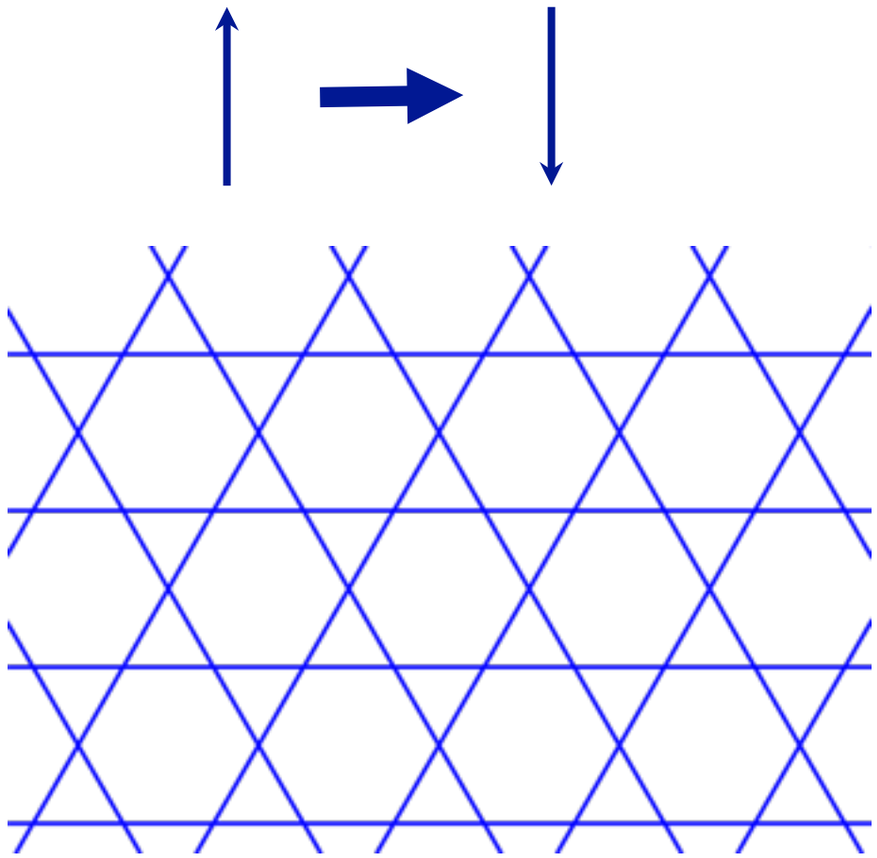

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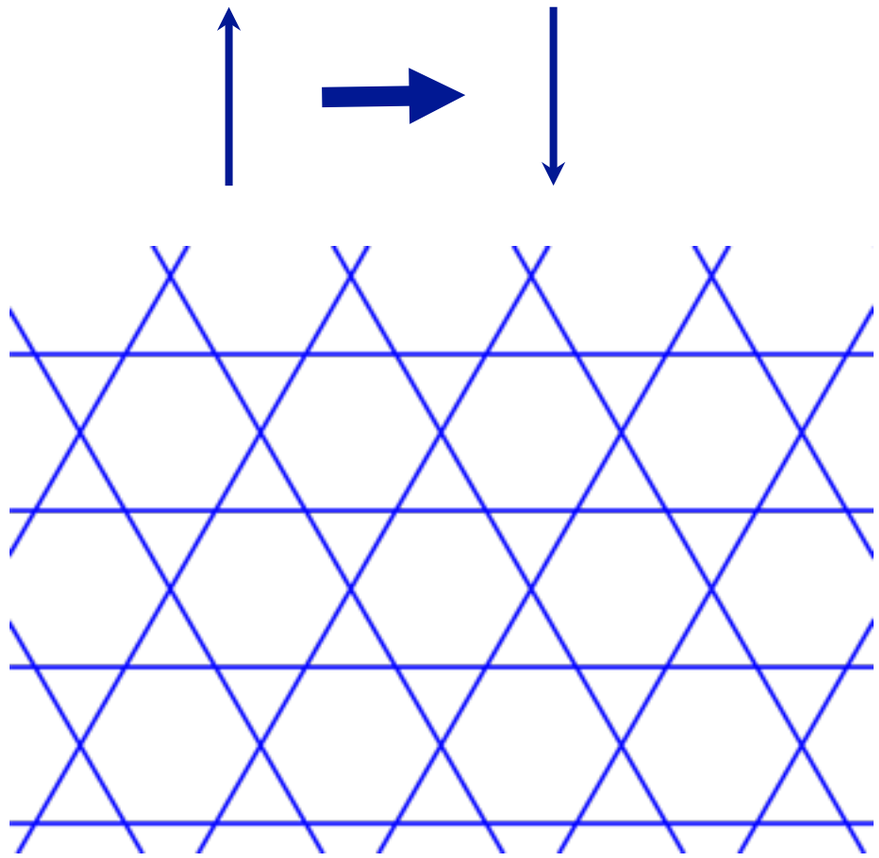

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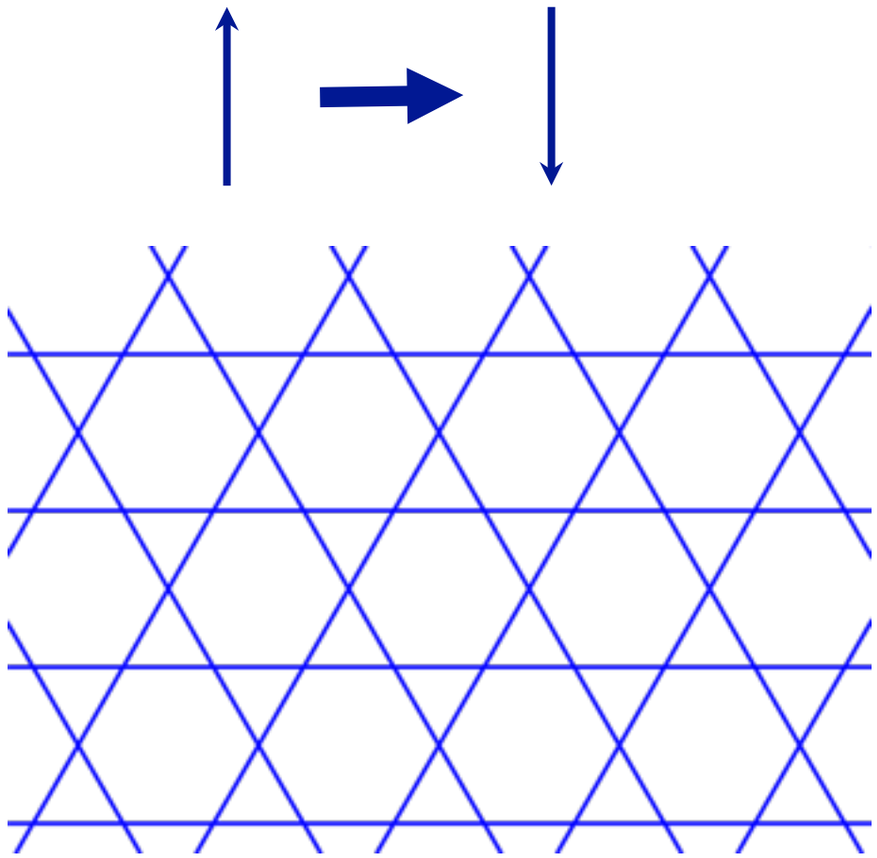
- Symmetries considered in some models: smaller complexity at cost of more communication



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Loop for MAX_ITER
- **Reduction B** (MPI_Reduce)
- **L3** (local work, normalize v1)
- **Loop over rounds of msgs**
  - **MSG_NB** (MPI_Isend,upc_memput(_nbi))
  - **L4** (work on local matrix, only 1st iteration)
  - **SYNC** (no-op, upc_fence)
  - **L7** (manage msg reception and do remote work)
- **L8** (local work, A norm)
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Code structure

```
void execute(ed){
  L1: for (i=0; i<2^(n-m); i++)
        b += v1[i]*v1[i]
  L2: for(iter=0; iter<max_iters; iter++)
        MPI_Barrier
        MPI_Allreduce of b
      L3: for (i=0; i<2^(n-m); i++)                    L3
            v1[i] *= f1(iter,b)
      MPI_Isend/MPI_Irecv to vv1 using handler1
      // local contribution, no comm
      L4: for (i=0; i<2^(n-m); i++)                    L4
            v2[i] = a(i)*v1[i]
          L5: for (k=0; k<n-m; k++)
                v2[i] += g*v1[f2(i,k)]
      // remote contribution, comm
      L6: for (k=n-m; k<n; k++) // m iterations         L6
        MPI_Isend/MPI_Irecv to vv2 using handler2
        MPI_Wait on handler1
        L7: for (i=0; i<2^(n-m); i++)
              v2[i] += g*vv1[i]
        swap(vv1,vv2) // Pointer swap, no memcpy
        handler1 = handler2
      L8: for(i=0; i<2^(n-m); i++)                     L8
            a += v1[i]*v2[i]
        MPI_Barrier
        MPI_Allreduce of a
      L9: for(i=0; i<2^(n-m); i++)                     L9
            v2[i] = f3(i,iter,a)
            b += v2[i]*v2[i]
        swap (v0,v1,v2)
}
```

execute

SPIN single core/socket/node comparisons

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- Task-based OpenMP/MPI implementation by Fourestey/Stringfellow

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Sockets/Node	2	2	2
Hyperthreading	no	unenabled	yes (2)
Compiler	Open64	Intel	Intel
Core time (s.)	754 (1T)	280 (1T)	227 (1T)
Socket time (s.)	74 (15T)	51 (6T)	29 (16T)
Node time (s.)	38 (31T)	26 (12T)	15 (32T)

Multi-buffering concept

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Double buffering

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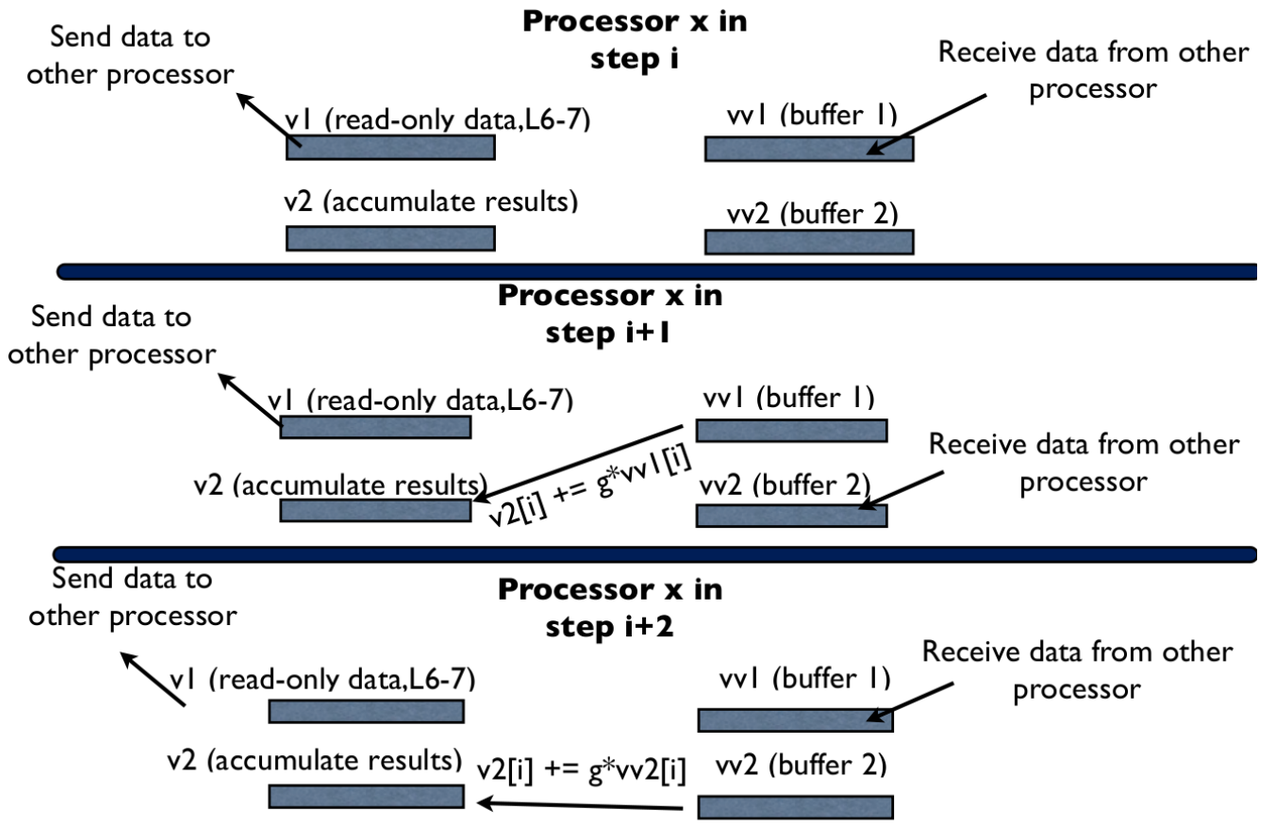

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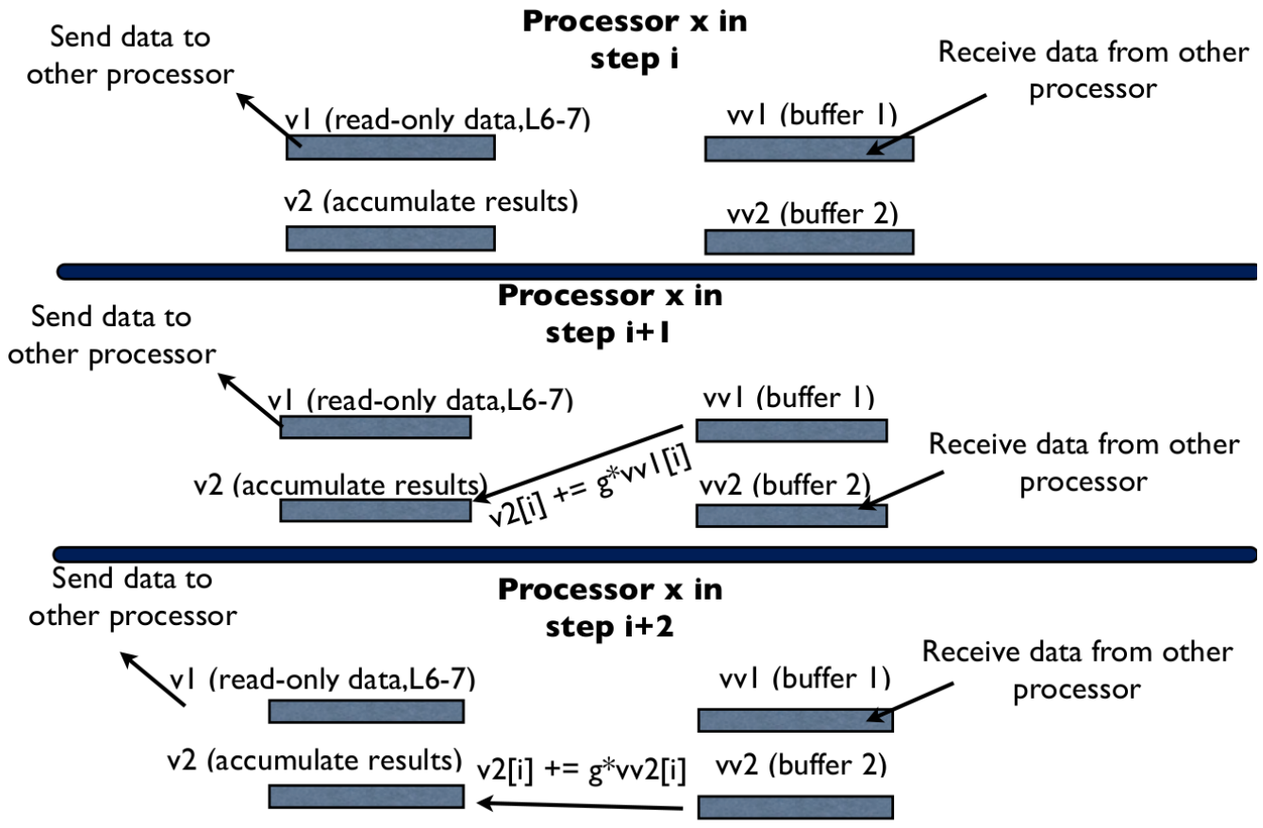

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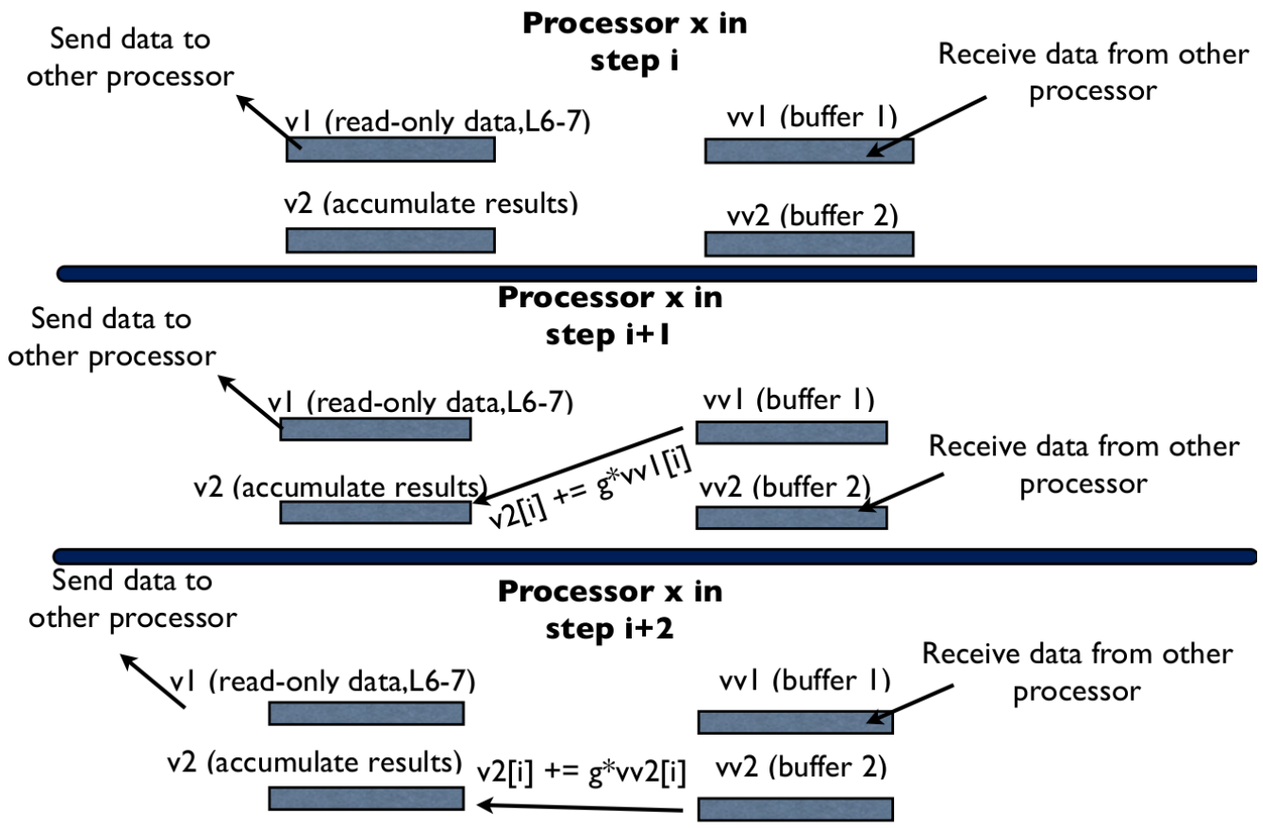

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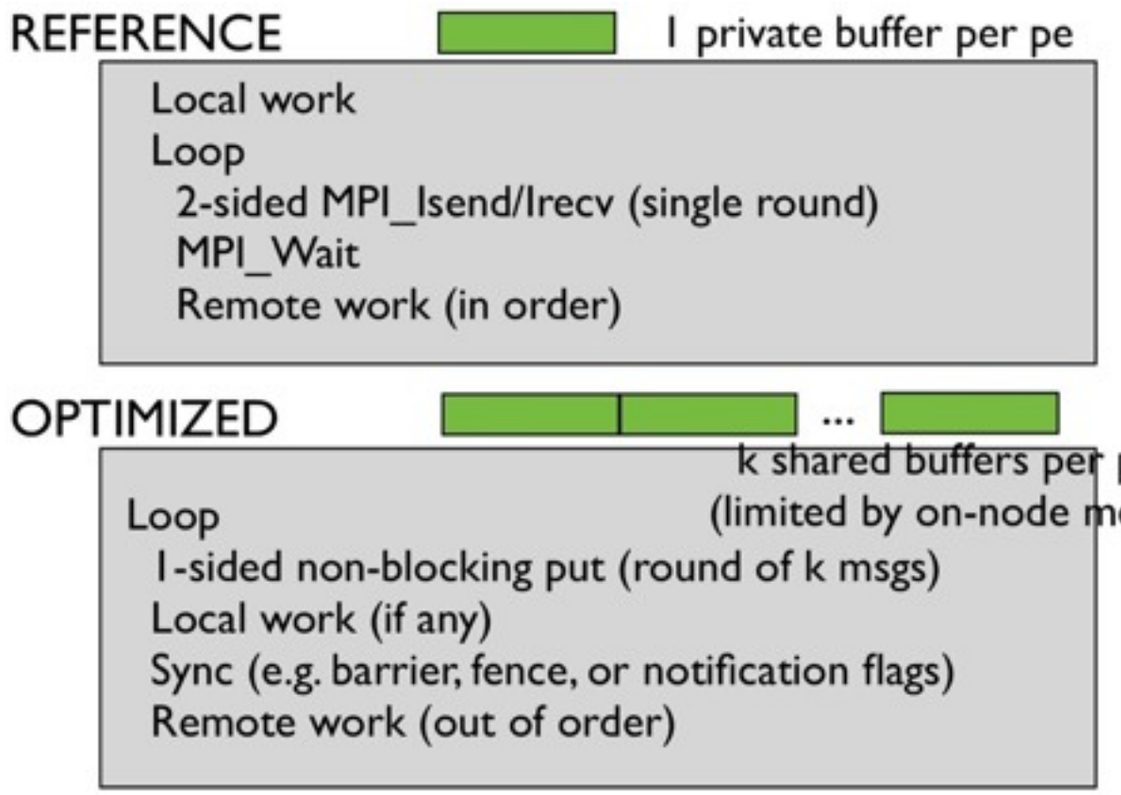

UPC “Elegant” Implementation

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```
struct ed_s { ...
        shared double *v0, *v1, *v2;        /* vectors */
        shared double *swap;                /* for swapping vectors */
};
                :
for (iter = 0; iter < ed->max_iter; ++iter) {
                  :
                upc_barrier(0);
                /* matrix vector multiplication */
                upc_forall (s = 0; s < ed->nlstates; ++s; &(ed->v1[s]) ) {
                        /* diagonal part */
                        ed->v2[s] = diag(s, ed->n, ed->j) * ed->v1[s];
                        /* offdiagonal part */
                        for (k = 0; k < ed->n; ++k) {
                                s1 = flip_state(s, k);
                                ed->v2[s] += ed->gamma * ed->v1[s1];
                        }
                }
                 :
                /* Calculate alpha */
                /* Calculate beta */
        }
}
```

Inelegant **UPC versions**

Inelegant UPC versions

Inelegant 1

```
shared[NBLOCK] double vtmp[THREADS*NBLOCK];
  :
for (i = 0; i < NBLOCK; ++i) vtmp[i+MYTHREAD*NBLOCK] = ed->v1[i];
upc_barrier(1);
for (i = 0; i < NBLOCK; ++i) ed->vv1[i] = vtmp[i+(ed->from_nbs[0]*NBLOCK)];
  :
upc_barrier(2);
```

Inelegant 2

```
shared[NBLOCK] double vtmp[THREADS*NBLOCK];
  :
upc_memput( &vtmp[MYTHREAD*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
upc_barrier(1);
upc_memget( ed->vv1, &vtmp[ed->from_nbs[0]*NBLOCK], NBLOCK*sizeof(double) );
  :
upc_barrier(2);
```

UPC *Inelegant3:* use double buffers and upc_put

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```
shared[NBLOCK] double vtmp1[THREADS*NBLOCK];
shared[NBLOCK] double vtmp2[THREADS*NBLOCK];
:
upc_memput( &vtmp1[ed->to_nbs[0]*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
upc_barrier(1);
:
 if ( mode == 0 ) {
   upc_memput( &vtmp2[ed->to_nbs[neighb]*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
 } else {
   upc_memput( &vtmp1[ed->to_nbs[neighb]*NBLOCK], ed->v1, NBLOCK*sizeof(double) );
 }
  :
if ( mode == 0 ) {
  for (i = 0; i < ed->nlstates; ++i) { ed->v2[i] += ed->gamma * vtmp1[i+MYTHREAD*NBLOCK]; }
  mode = 1;
} else {
  for (i = 0; i < ed->nlstates; ++i) { ed->v2[i] += ed->gamma * vtmp2[i+MYTHREAD*NBLOCK]; }
  mode = 0;
}
upc_barrier(2);
```

Other message passing paradigms

MPI-2: One-sided PUT

```
MPI_Put(ed->v1, ed->nlstates, MPI_DOUBLE, ed->to_nbs[0], 0, ed->nlstates, MPI_DOUBLE, win1);
MPI_Win_fence( 0, win1);
```

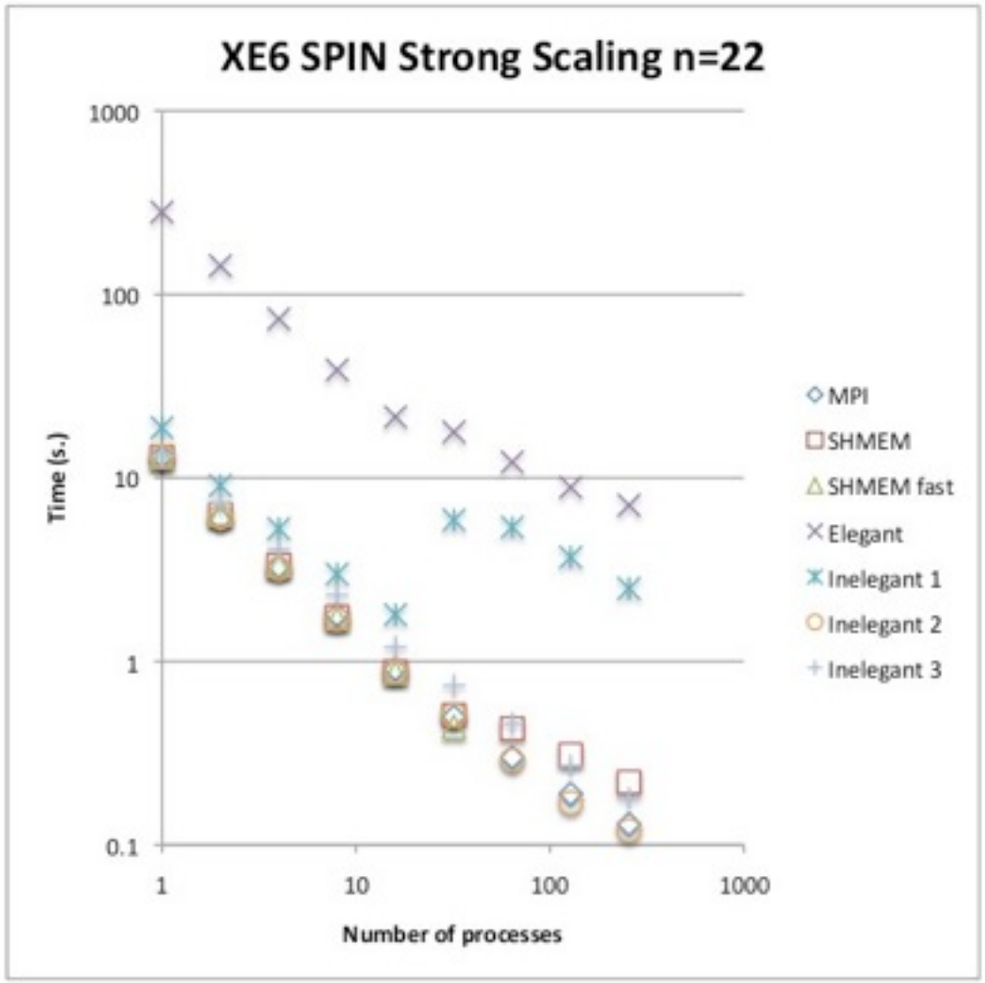
SHMEM: non-blocking PUT

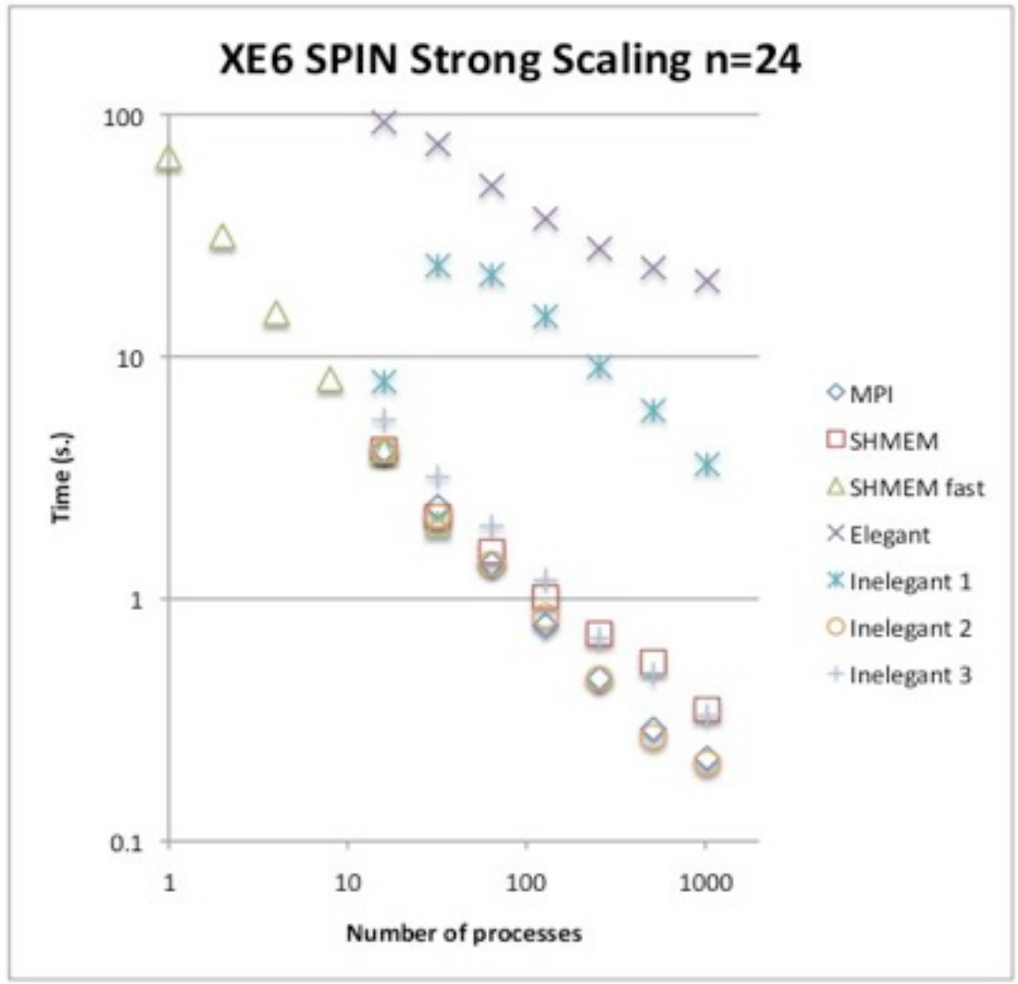
```
vtmp1 = (double *) shmalloc(ed->nlstates*sizeof(double));
  :
shmem_barrier_all();
shmem_double_put_nb(vtmp1, ed->v1, ed->nlstates, ed->from_nbs[neighb], NULL);
```

SHMEM "fast": non-blocking PUT, local wait only

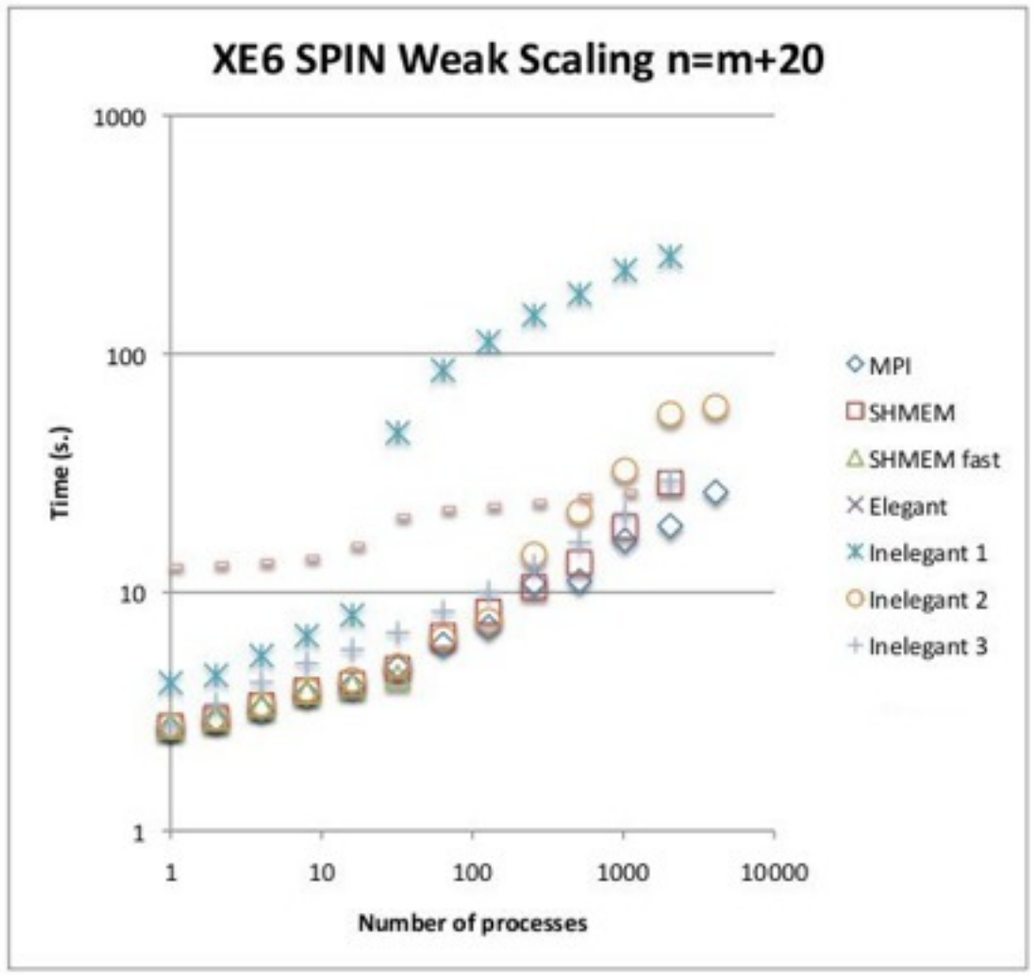
```
ed->v1[ed->nlstates] = ((double) ed->rank); /* sentinel */
for (l = 0; l < ed->m; ++l) {
  offset = l*(ed->nlstates+1); /* Offset into buffer */
  shmem_double_put_nb(&vtmp[offset],ed->v1, ed->nlstates+1,ed->to_nbs[l],NULL);
}
            :
tag = vtmp[offset+ed->nlstates];
while (tag != (double) ed->from_nbs[k-ed->nm]) { /* spin */
  tag = vtmp[offset+ed->nlstates];
}
for (i = offset, j=0; i < offset+ed->nlstates; ++i, ++j) {
   ed->v2[j] += ed->gamma * vtmp[i];
}
vtmp[l*(ed->nlstates+1)+ed->nlstates]=((double)-1); /*reset*/
```

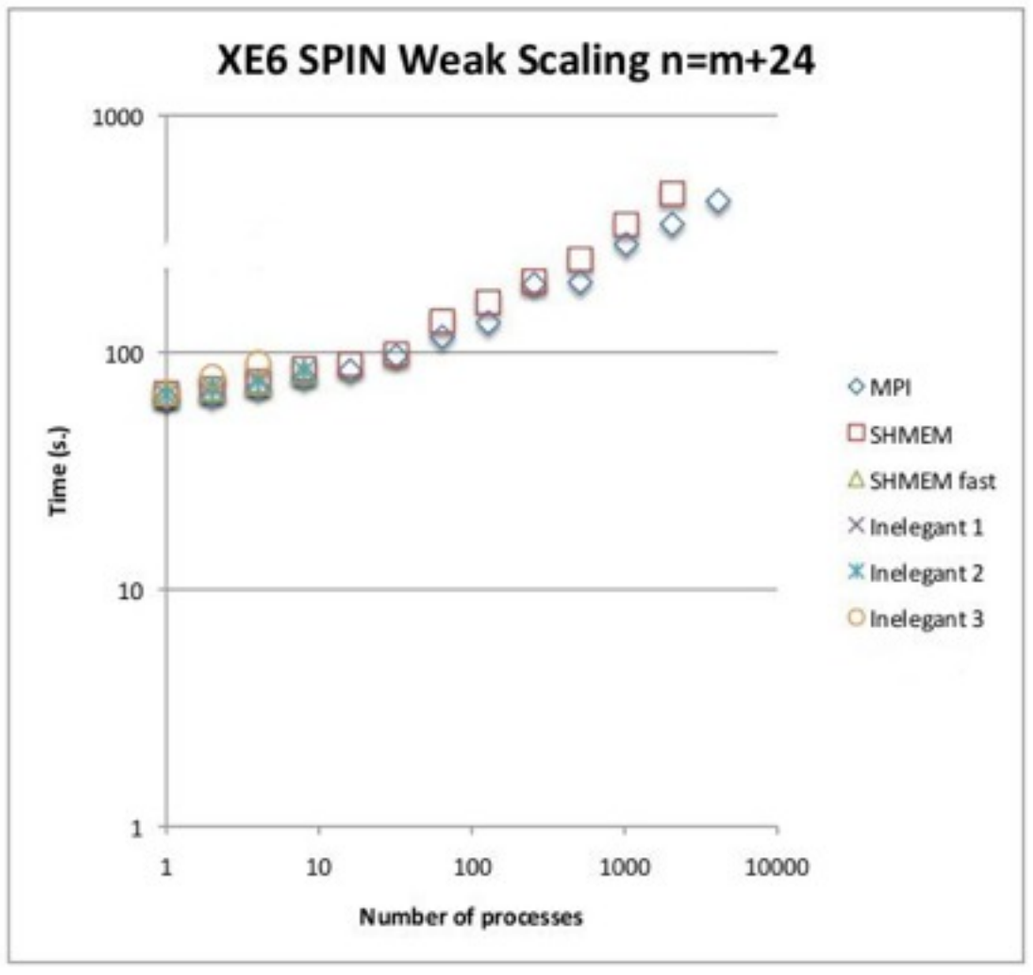
SPIN strong scaling: Cray XE6, n=22,24; 10 iter.





SPIN weak scaling: Cray XE6/Gemini, 10 iterations





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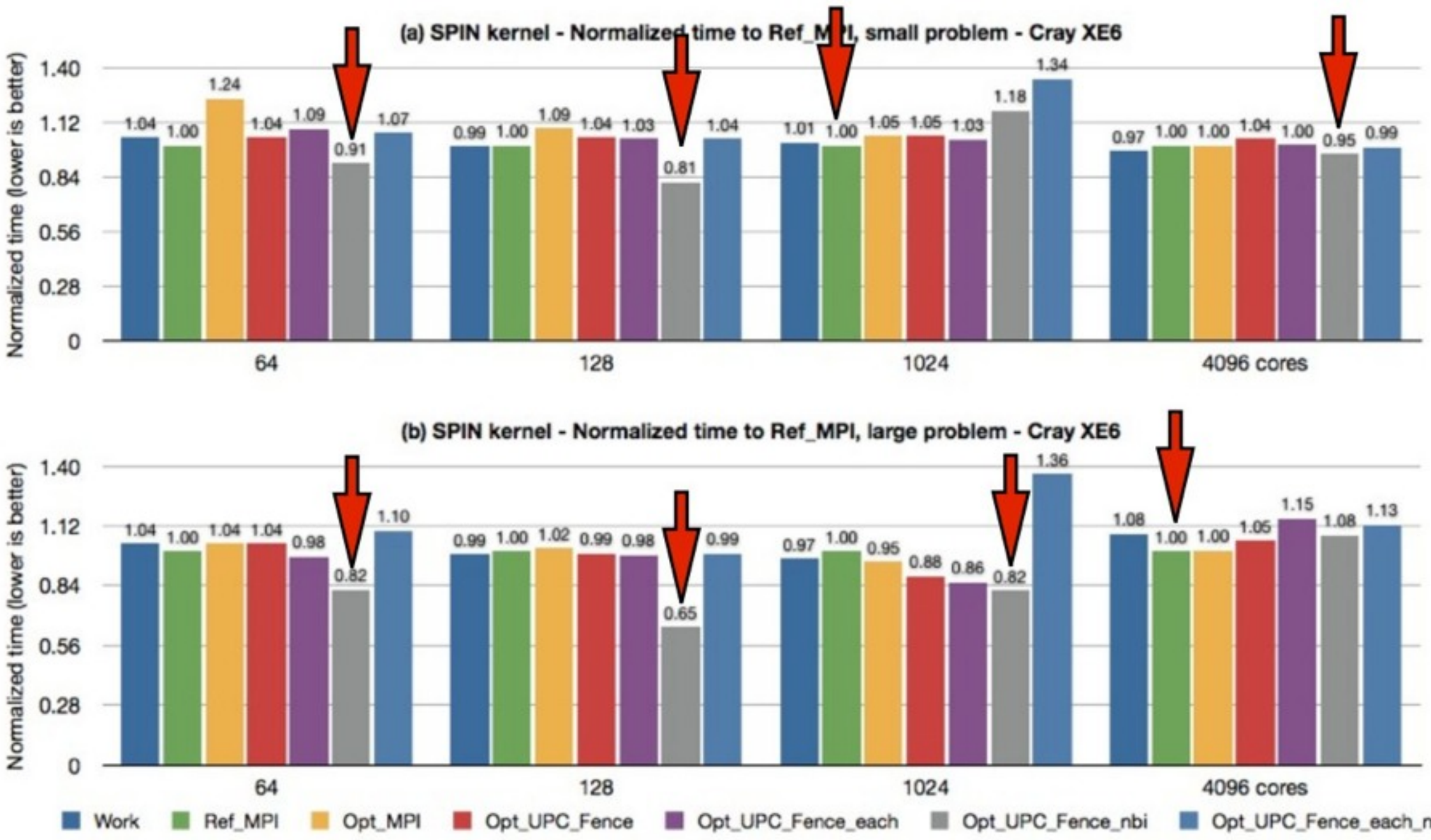

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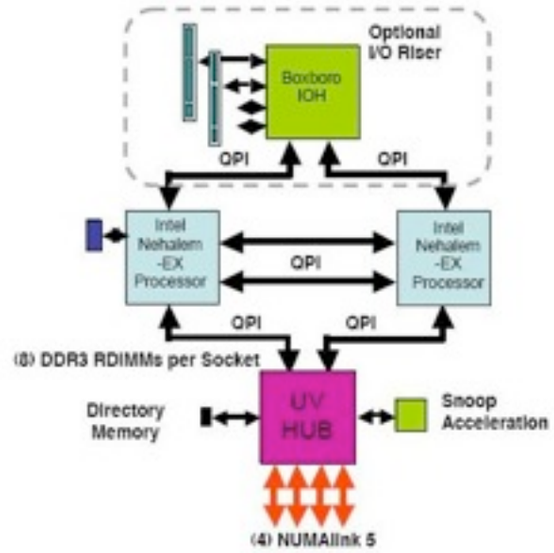

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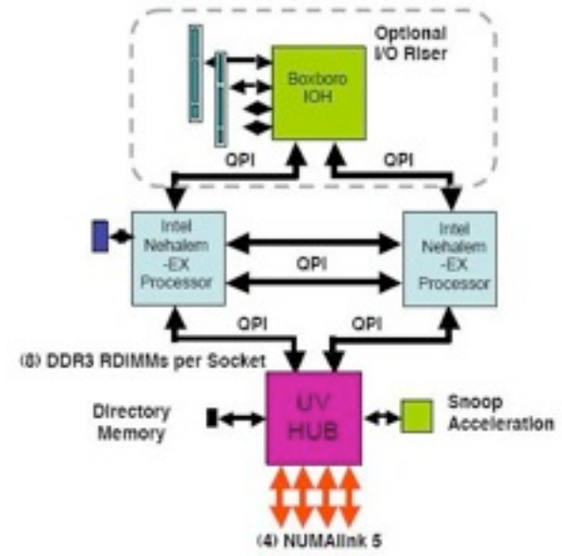

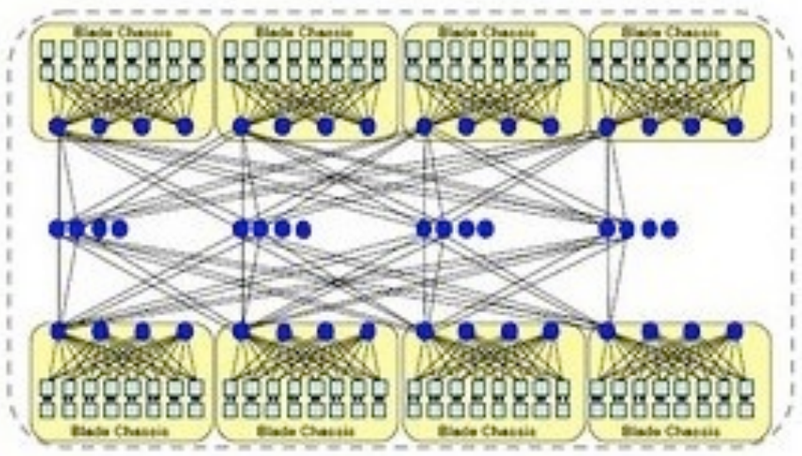

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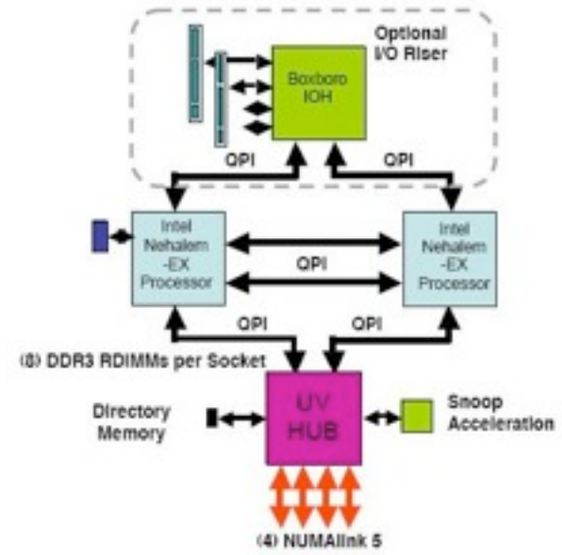

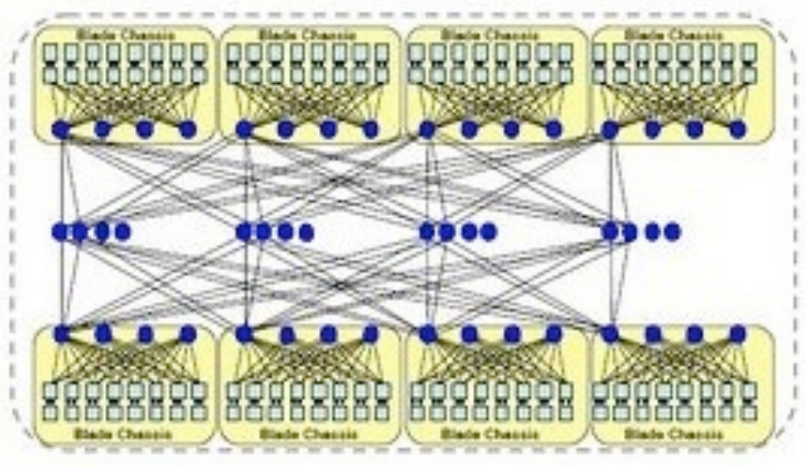

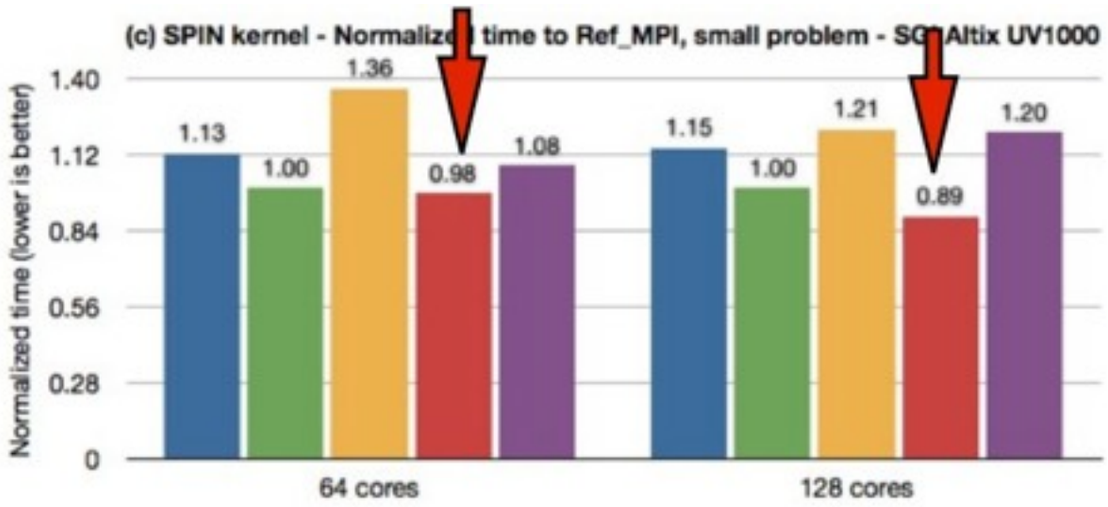

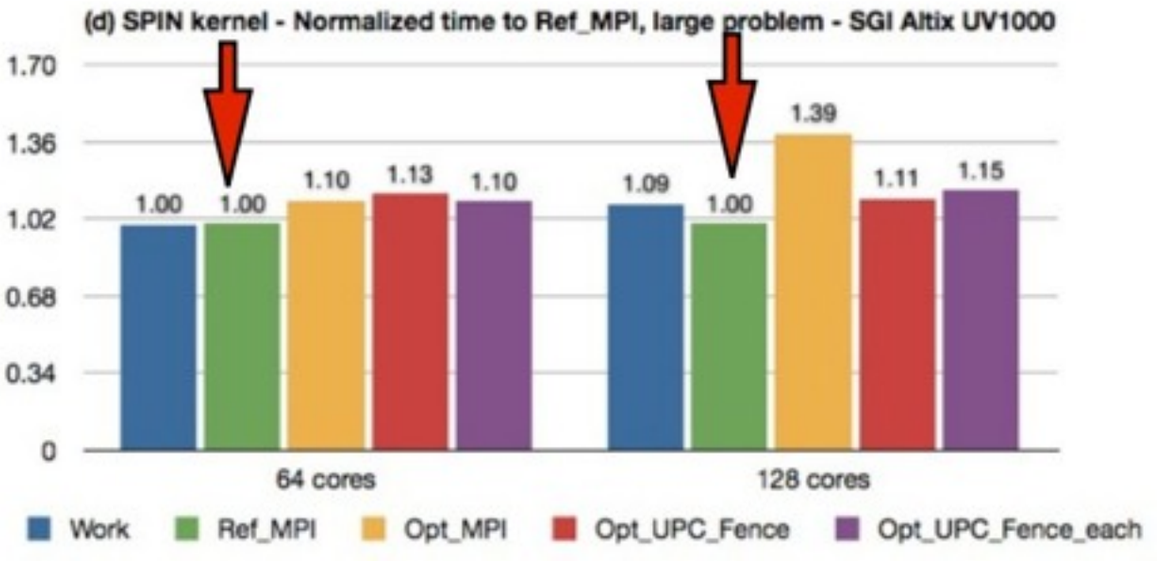

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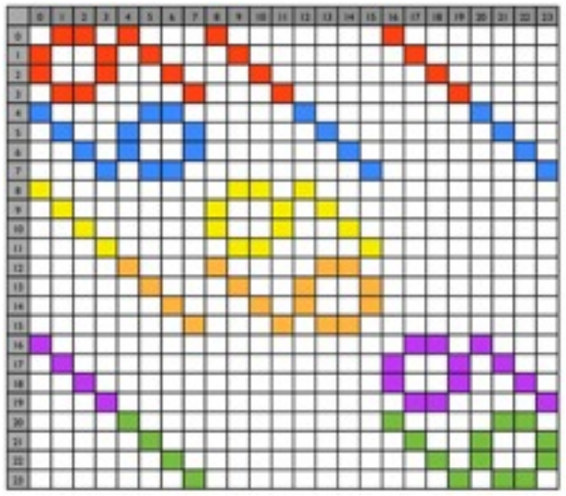

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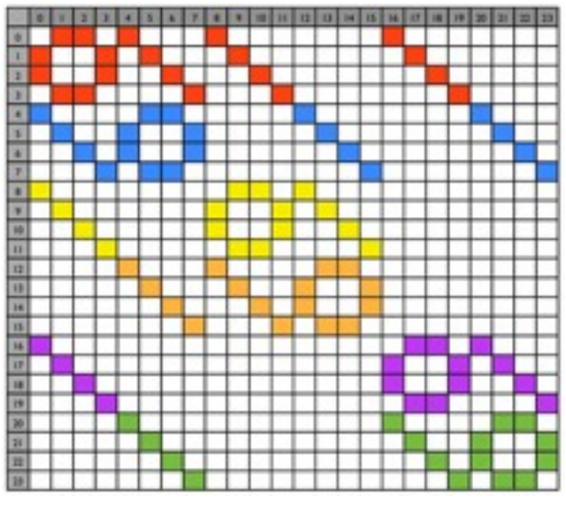

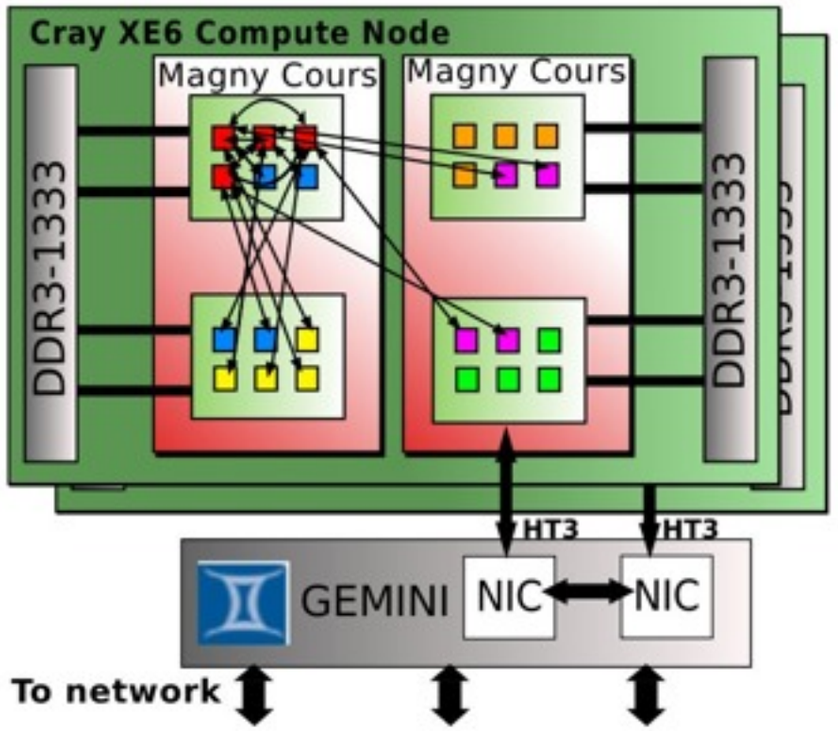

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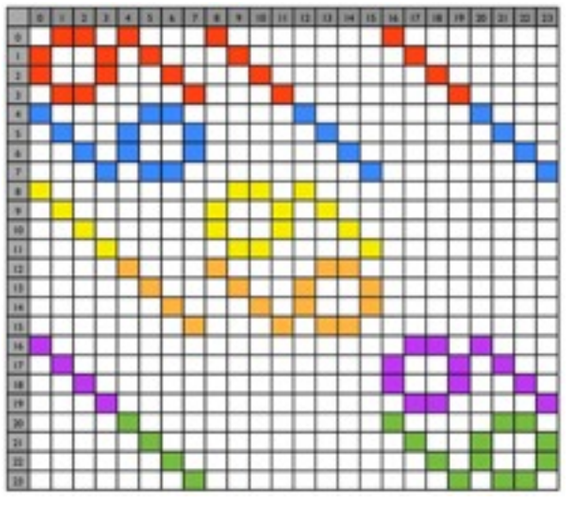

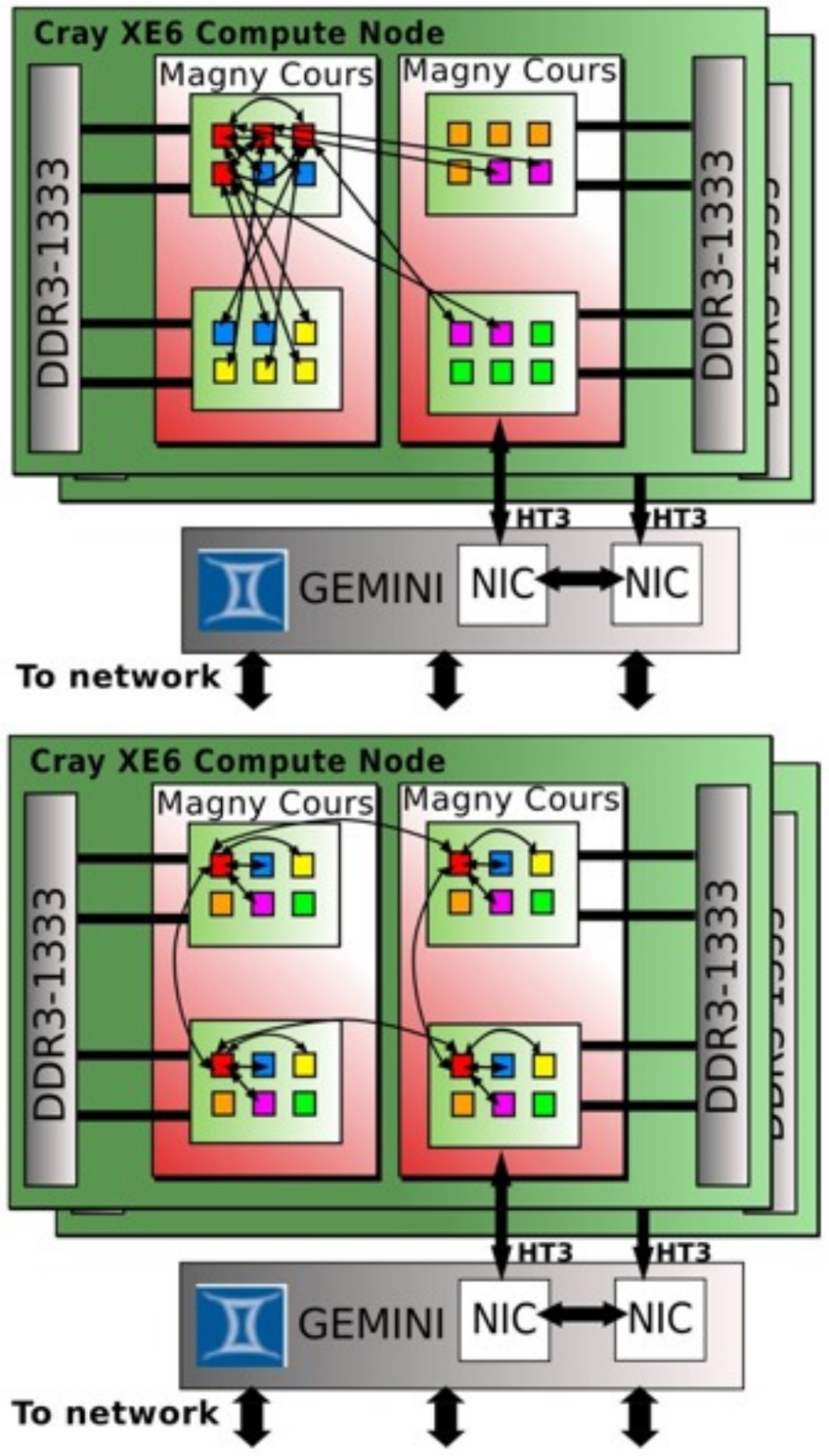

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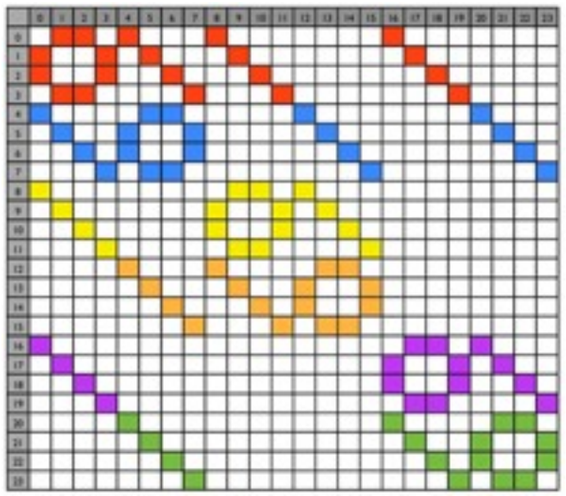

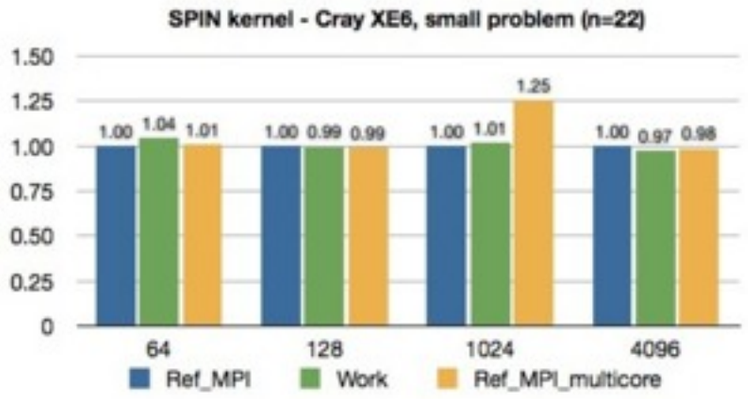

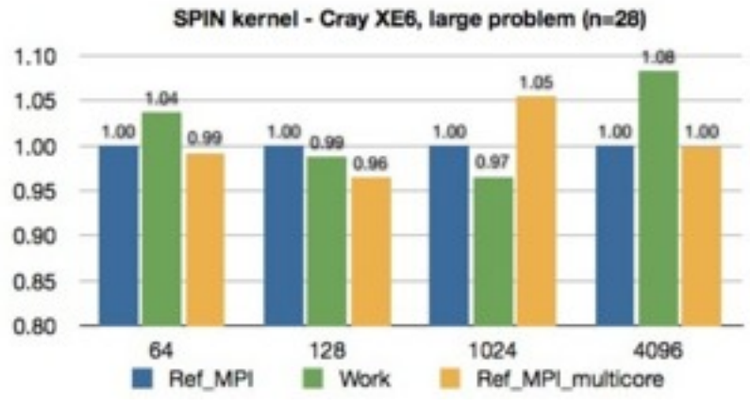

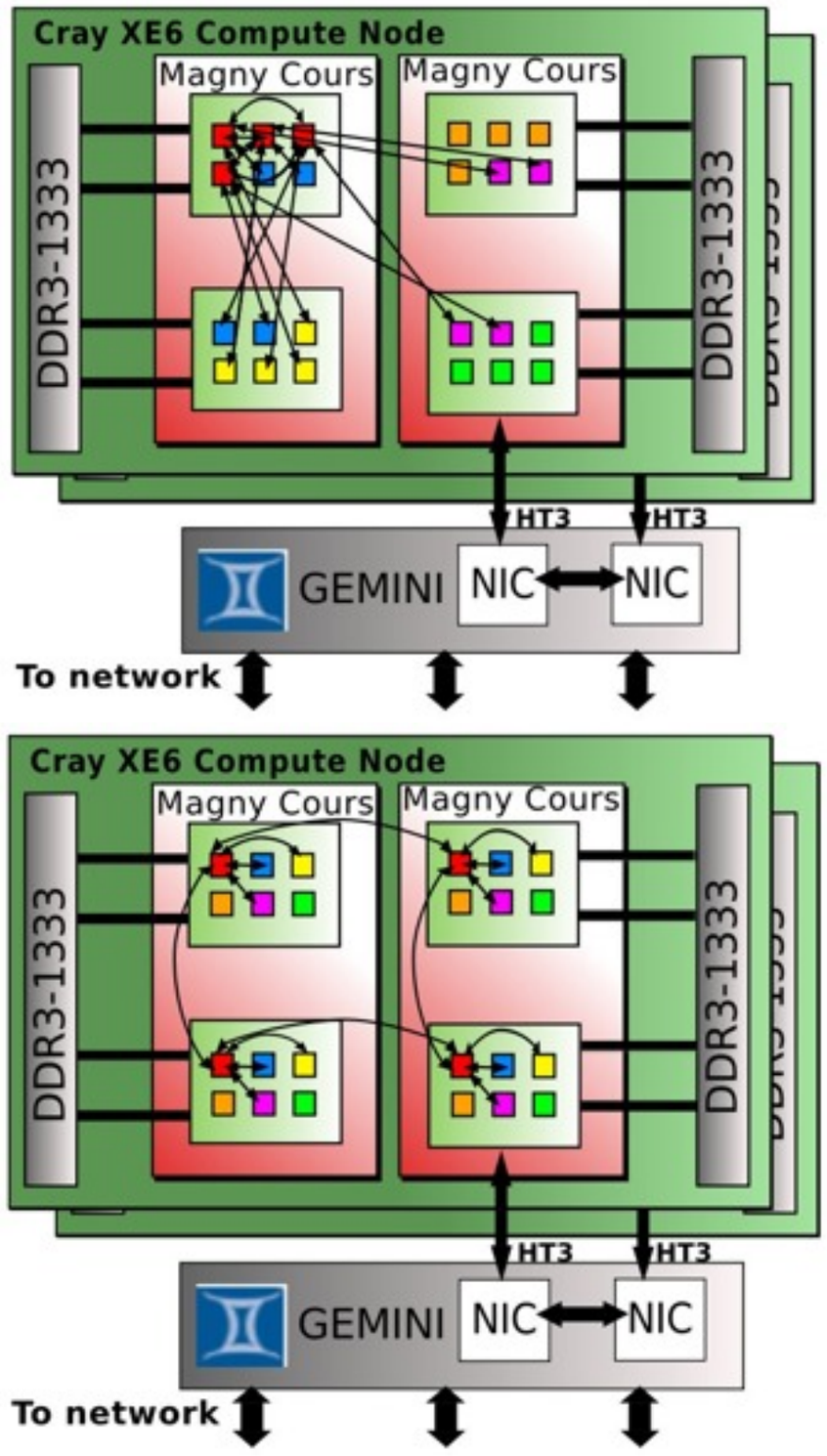

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MPI Processes	MPI-only (s.)	2 Threads (s.)	4 Threads (s.)
4096	17.4		
2048	28.1	16.6	
1024	48.9	25.1	14.4

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```
// local offdiagonal part
for (unsigned j = 0; j < asubspace.size(); ++j) {
    :
  index_type lastk = bspace.last(j);
  typename bspace_type::biterator it = bspace.begin(j);
#pragma omp parallel for
  for (index_type k = 0; k < lastk; ++k) {
    if (it[k].size == 0) continue;
    state_type state = it[k].state | a_state;
    value_type nv =
     matrix.def.b_apply(state, pvec, *this, ae, it[k].size);
    vspace.slice(rvec, j)[k] += nv;
  }
}
```

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4	0,1,2,3	1011	667
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8	cpu	960	433

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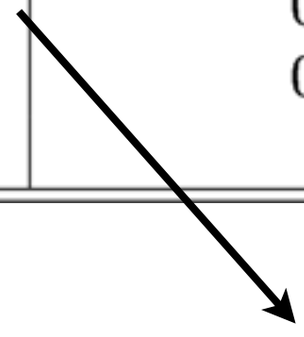

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- Cray bug reports filed, Cray has reproduced problem, working on optimizer

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PAPI_L2_TCM	821'641'494	80'416'142

Optimal # threads / socket

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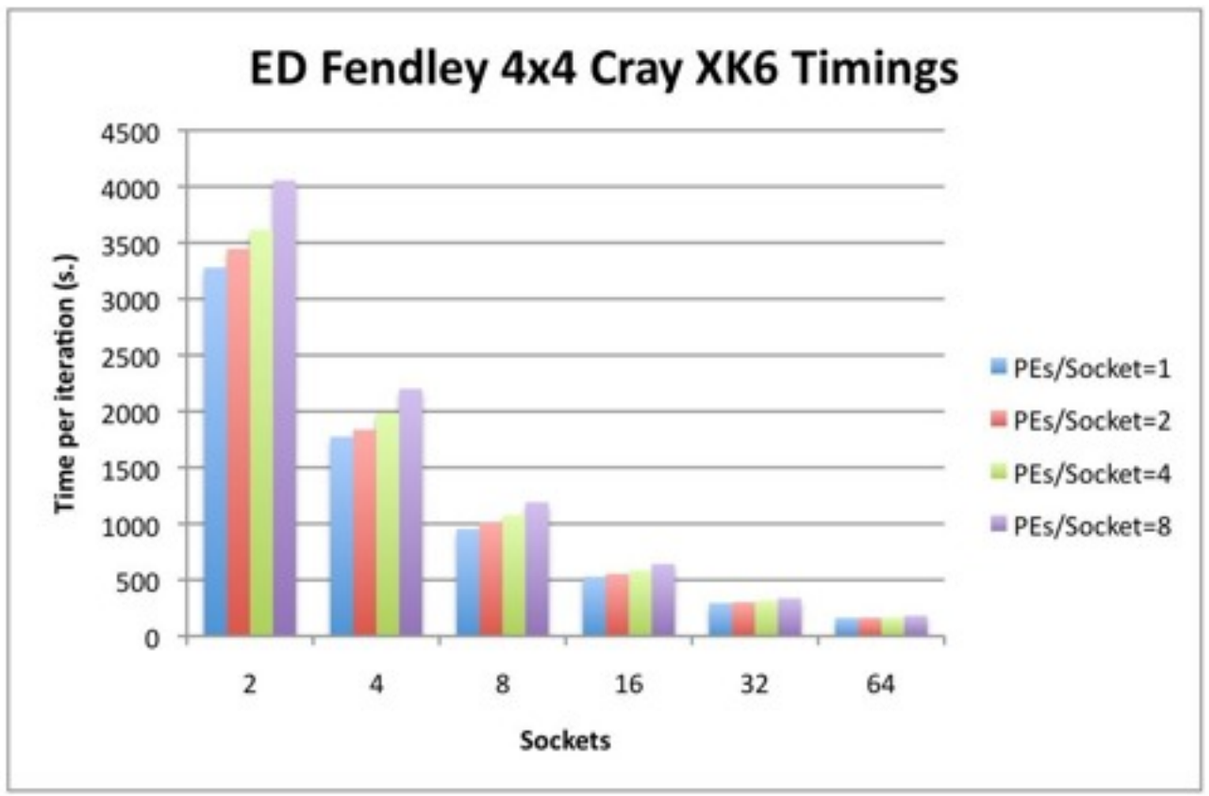

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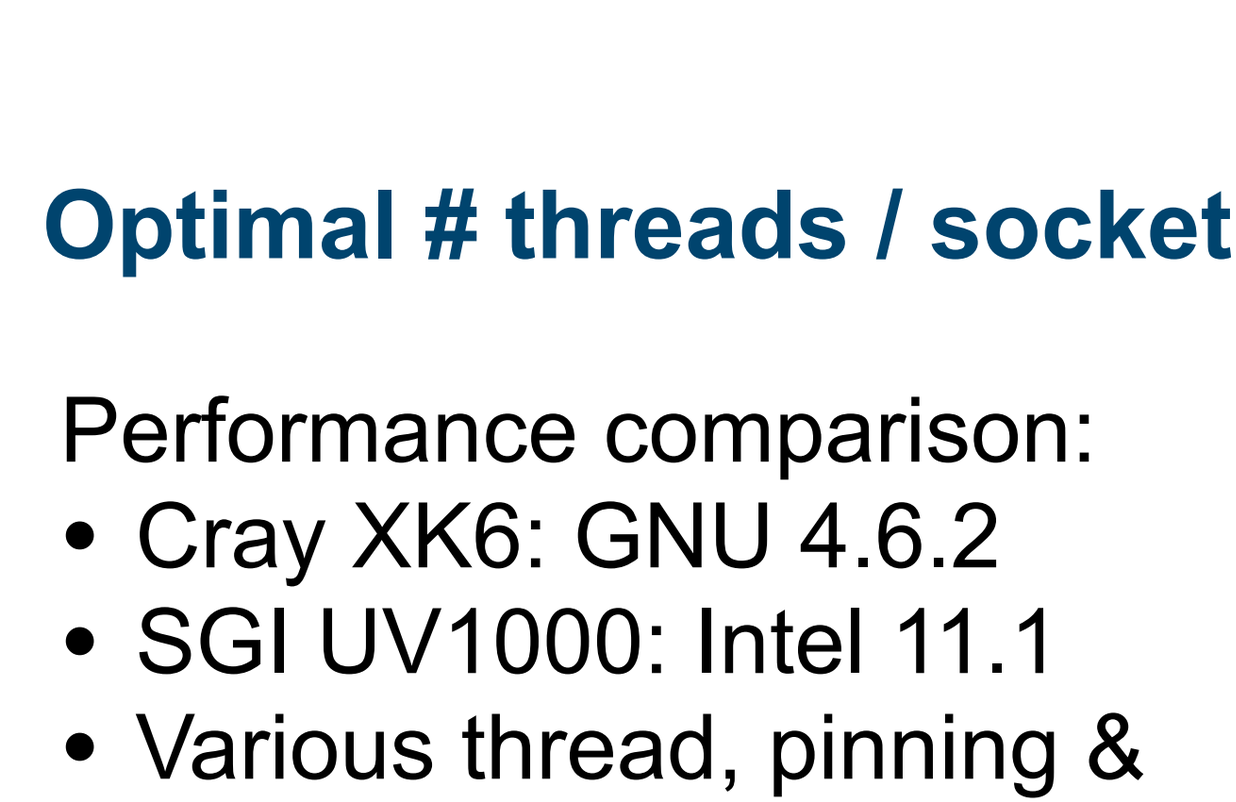

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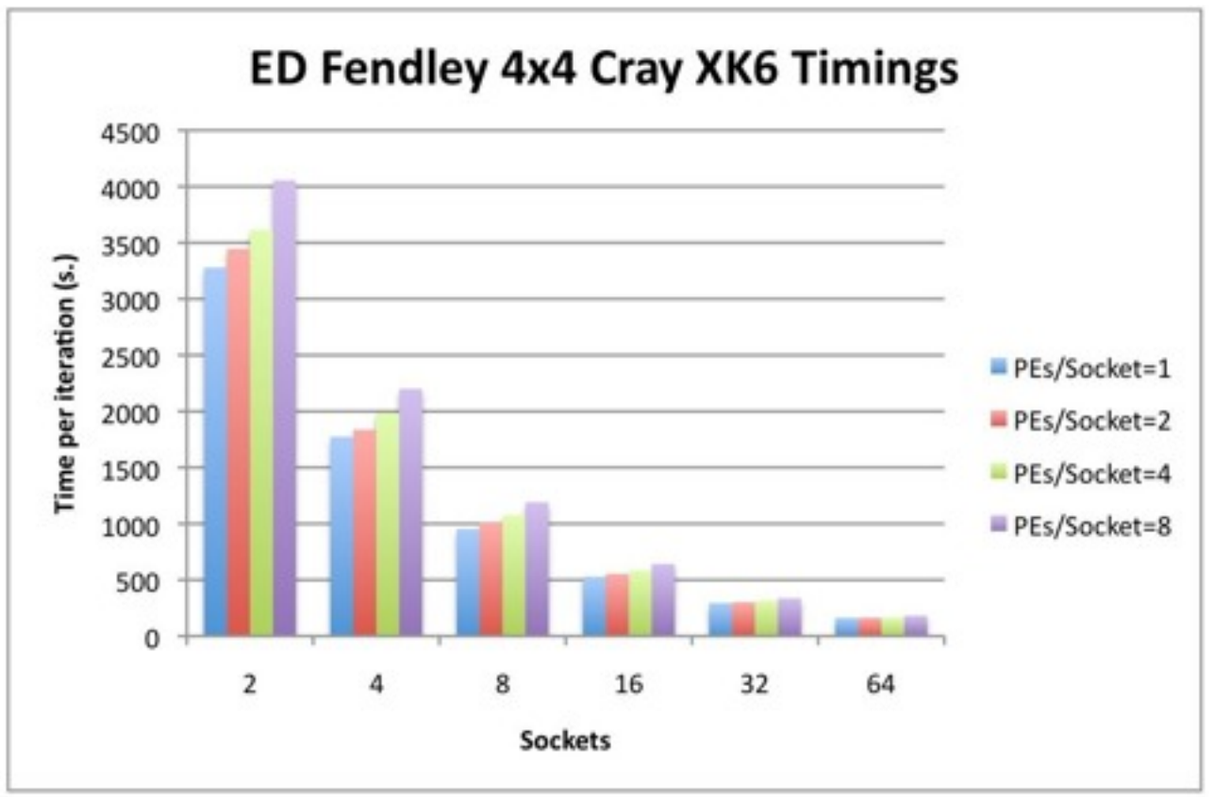

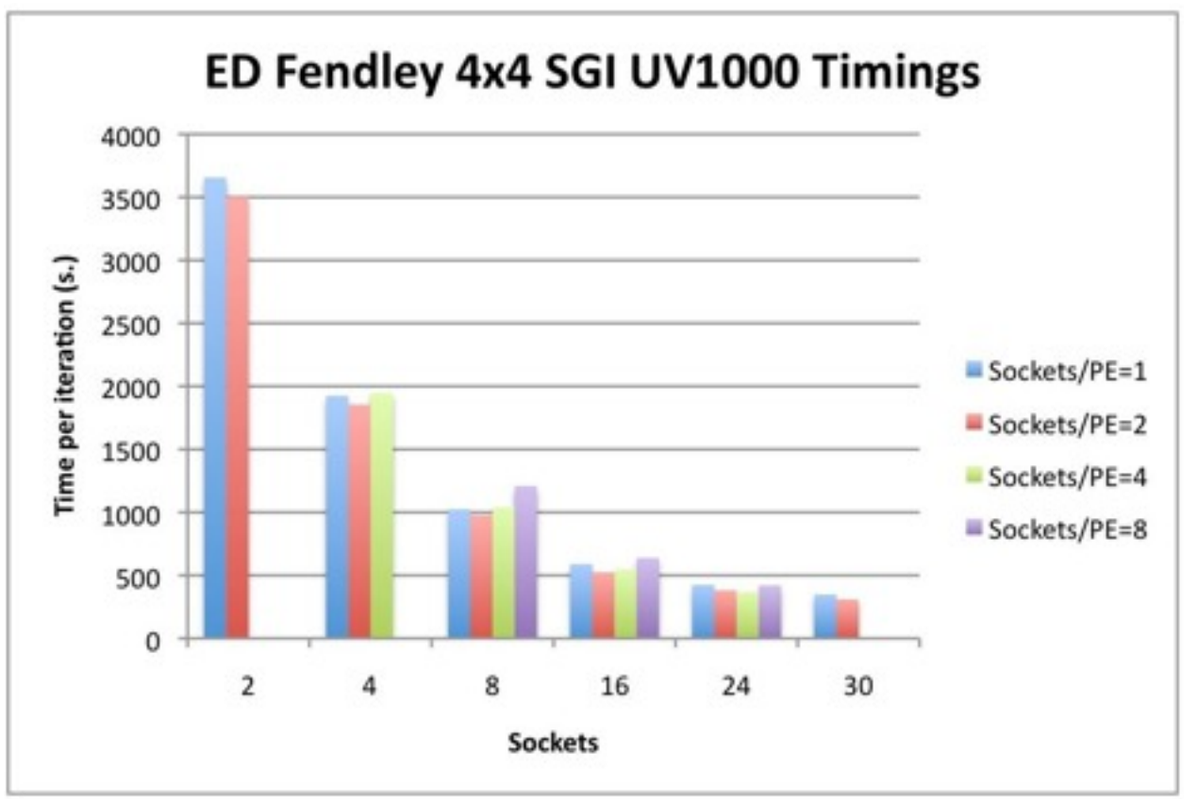

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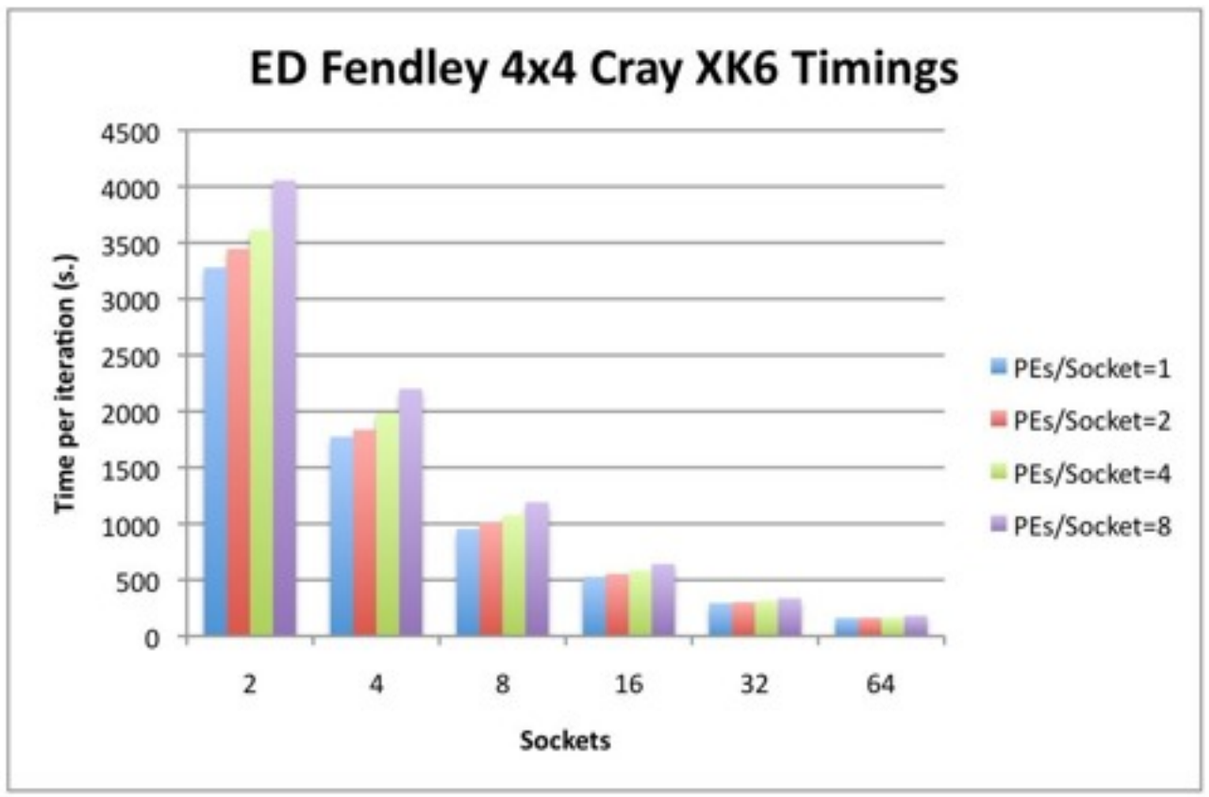

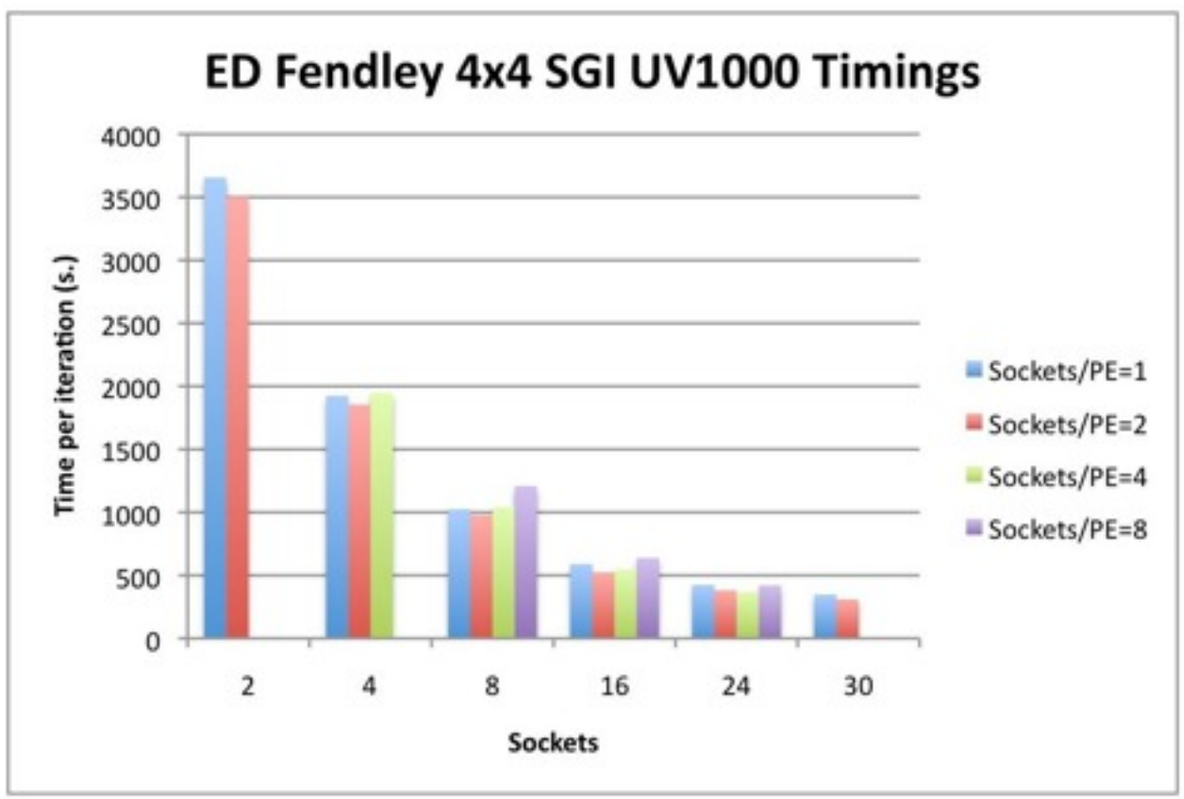

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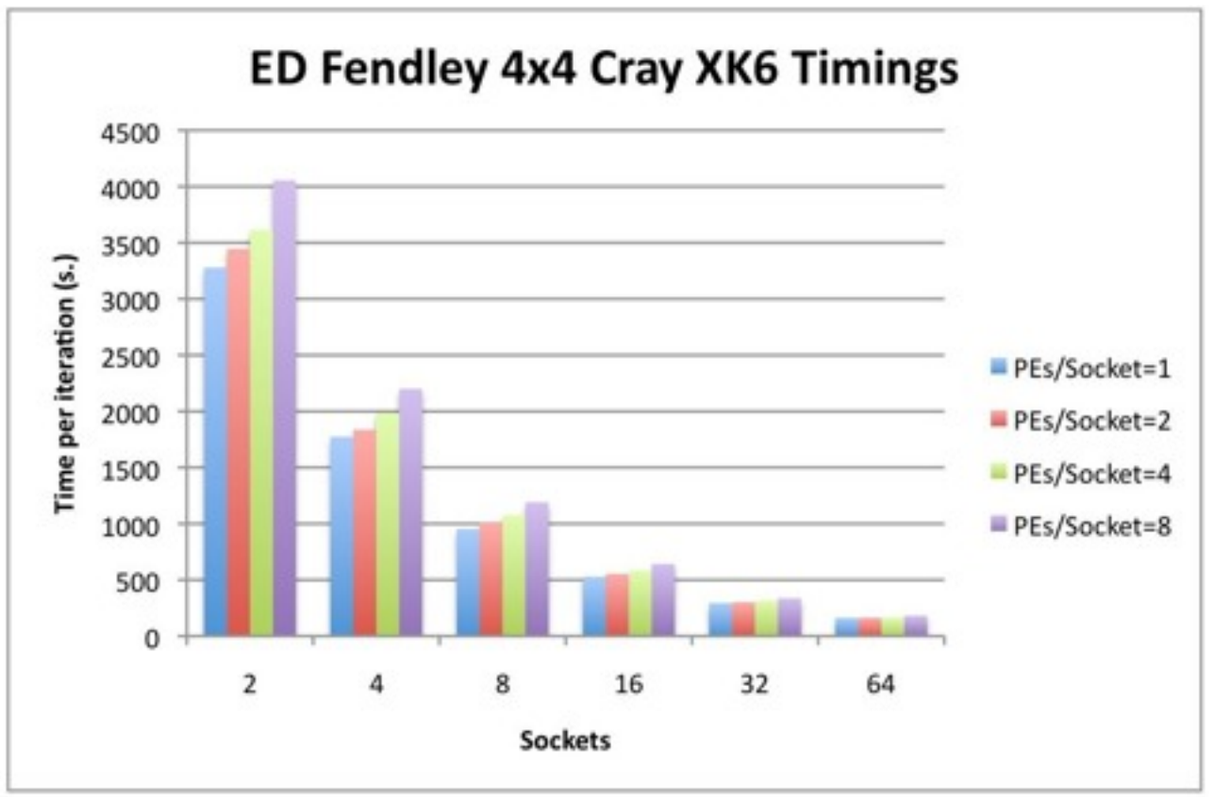
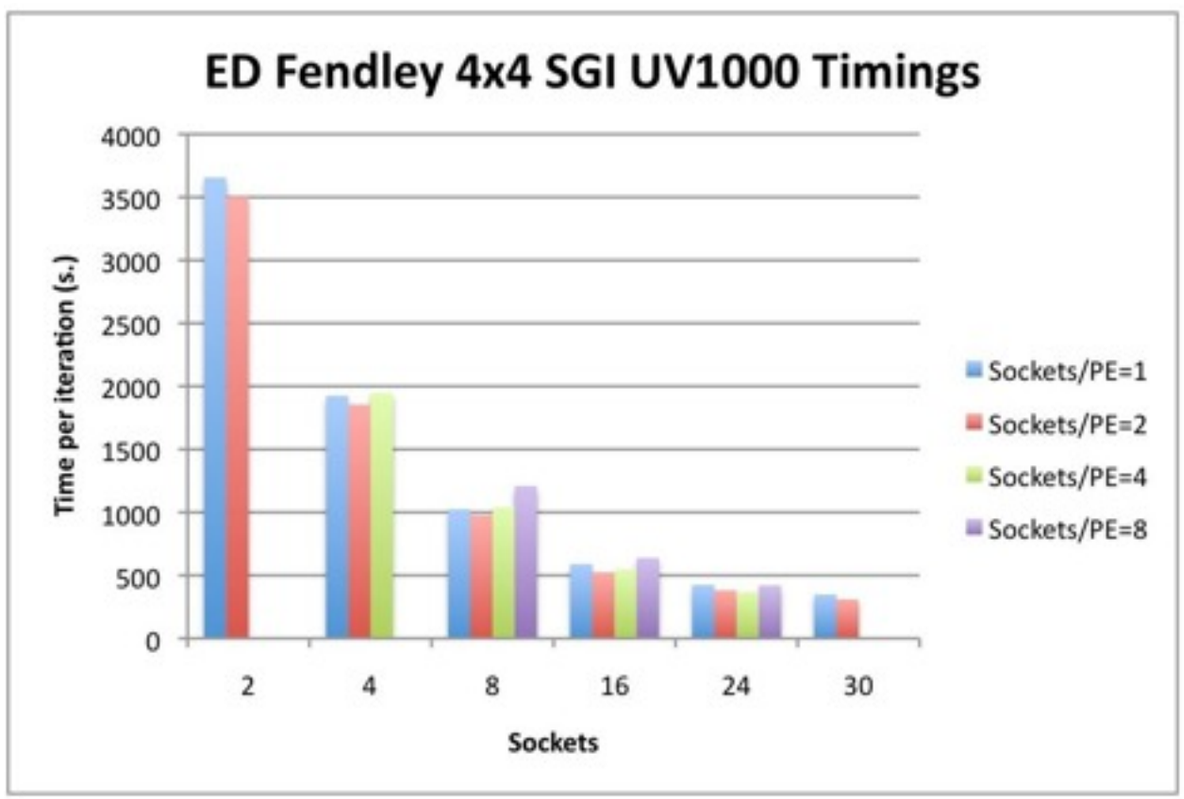
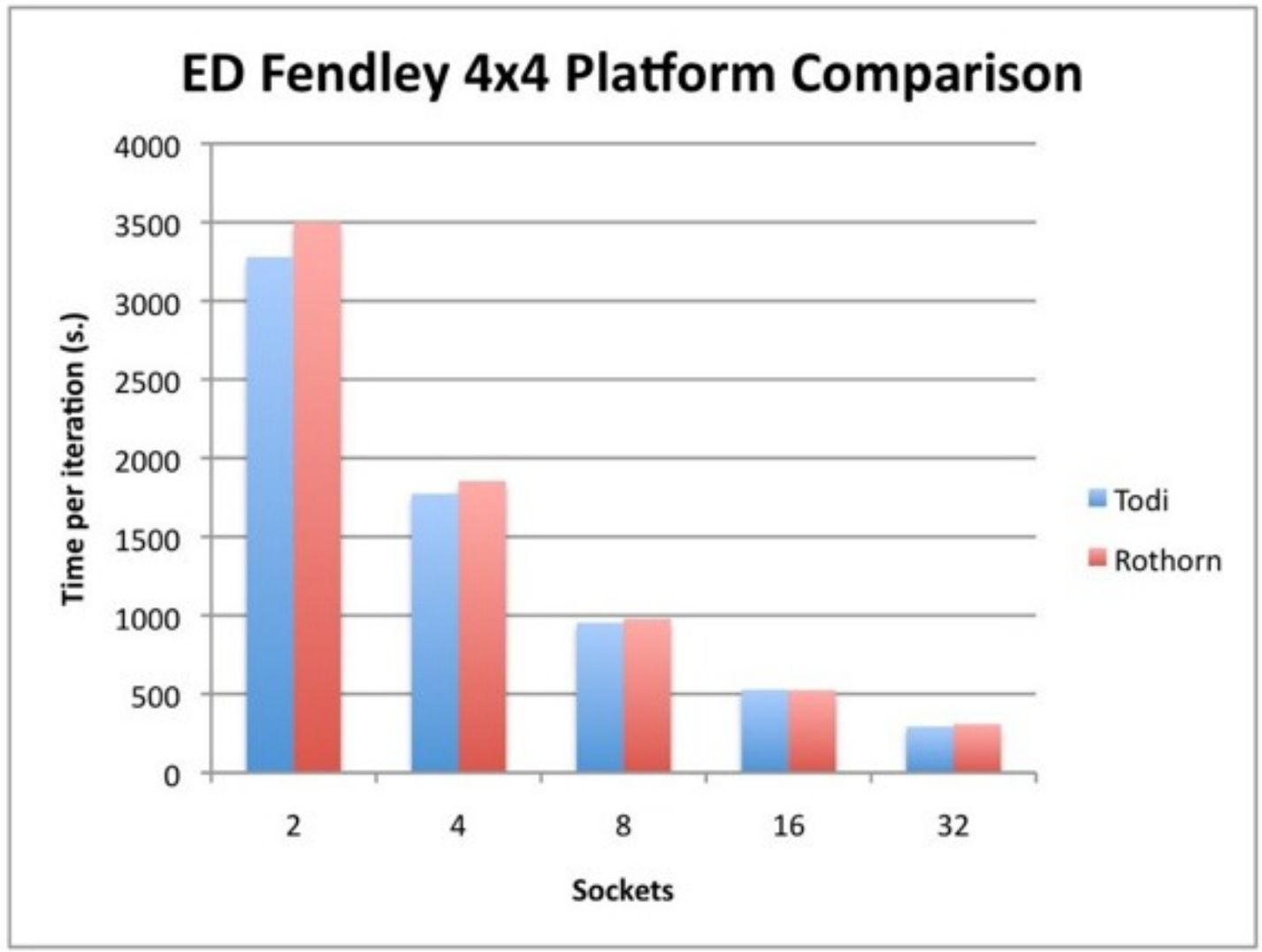
- SGI UV1000: 2 sockets / MPI Process, 16 threads





Performance Comparison Cray XE6 / SGI UV1000

- Cray XE6: AMD Interlagos, Gemini, GNU 4.6.2
- SGI UV1000: Intel Westmere, NUMAlink, Intel 11.1



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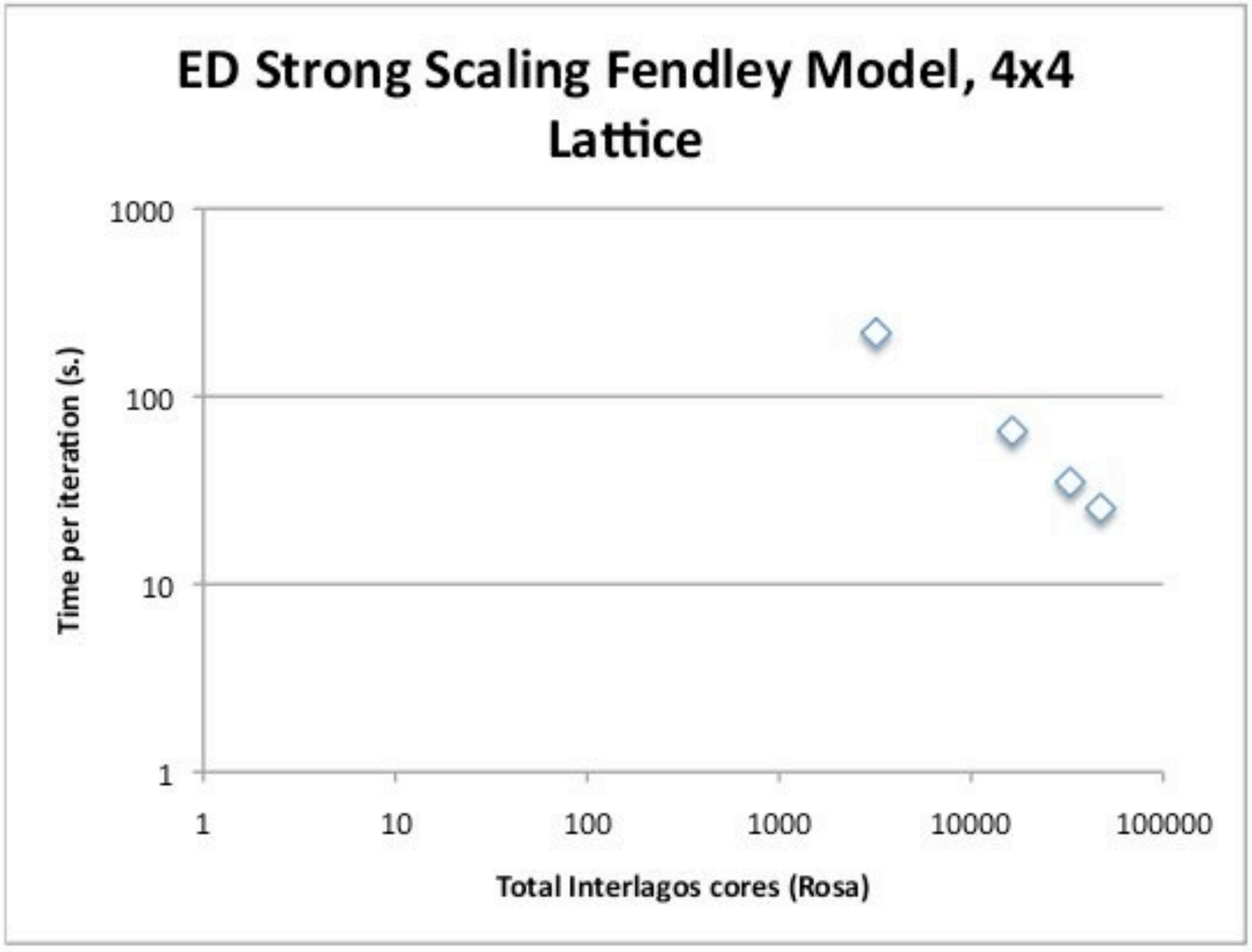

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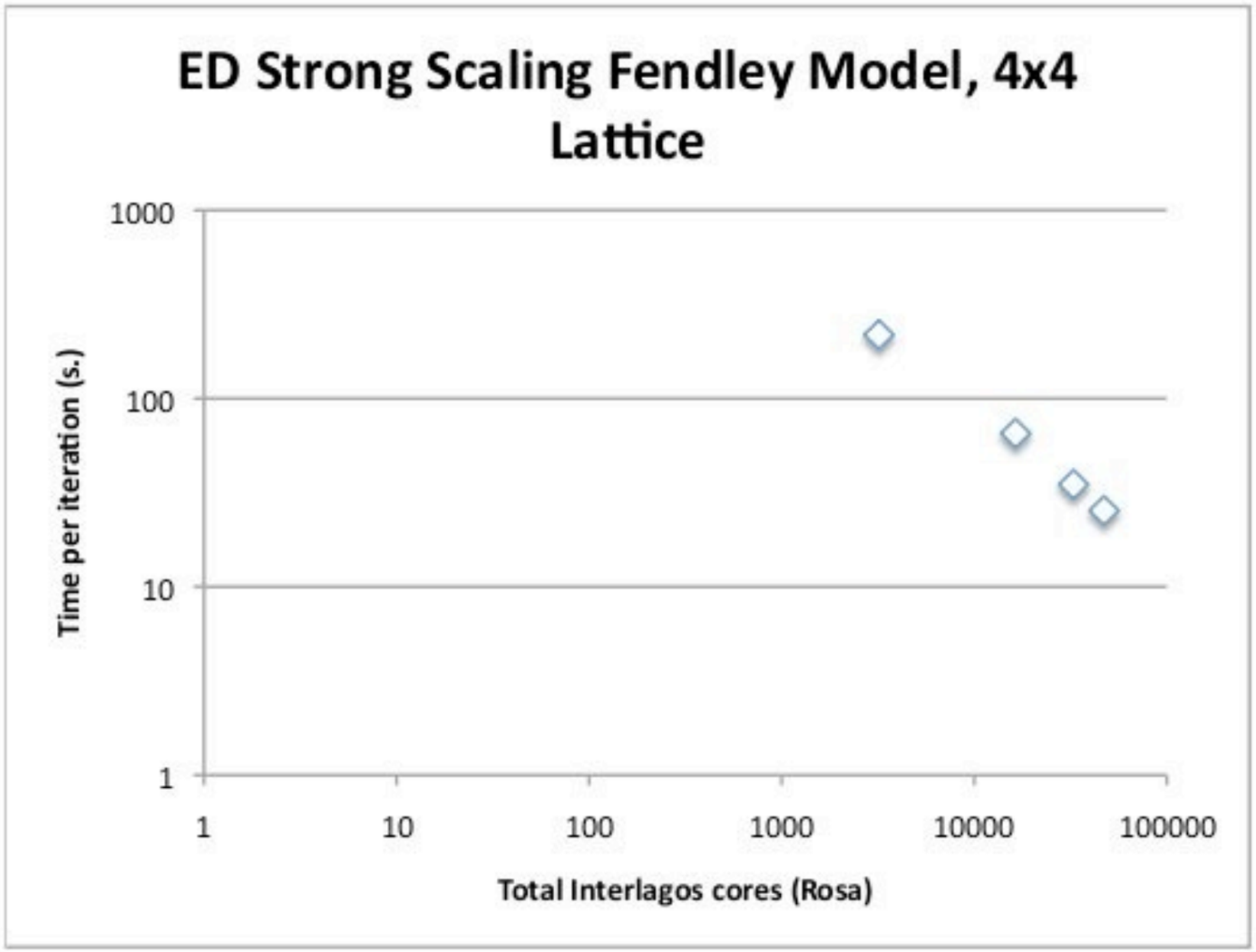

MPI Processes	Total Cores	Time/iteration (s.)
100	3200	218
512	16384	65.4
1024	32768	35
1476	47232	25.4

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Thank you for your attention!

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