High Performance Programming for Intel® Xeon Phi™ and Intel® Xeon® Products
Parallel Processing for Unparalleled Discovery

Jim Jeffers, Principal Engineer, Visualization Engineering Manager
Technical Computing Group, Intel Corporation
CUG 2014
It all comes down to PARALLEL PROGRAMMING!
(applicable to processors and Intel® Xeon Phi™ coprocessors both)

Forward, Preface
Chapters:
1. Introduction
2. High Performance Closed Track Test Drive!
3. A Friendly Country Road Race
4. Driving Around Town: Optimizing A Real-World Code Example
5. Lots of Data (Vectors)
6. Lots of Tasks (not Threads)
7. Offload
8. Coprocessor Architecture
9. Coprocessor System Software
10. Linux on the Coprocessor
11. Math Library
12. MPI
13. Profiling and Timing
14. Summary
Glossary, Index

Available since mid-February 2013.

Learn more about this book:
lotsofcores.com

This book belongs on the bookshelf of every HPC professional. Not only does it successfully and accessibly teach us how to use and obtain high performance on the Intel MIC architecture, it is about much more than that. It takes us back to the universal fundamentals of high-performance computing including how to think and reason about the performance of algorithms mapped to modern architectures, and it puts into your hands powerful tools that will be useful for years to come.

—Robert J. Harrison
Institute for Advanced Computational Science, Stony Brook University

Intel® Xeon Phi™ Coprocessor High Performance Programming,
Jim Jeffers, James Reinders, (c) 2013, publisher: Morgan Kaufmann

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Agenda

Brief Intel® Xeon Phi™ Product Overview and Roadmap

Key Optimization Considerations for Intel Xeon Phi Coprocessors (and other Intel Architecture Processors)

Some Application Performance Examples
Intel® Xeon Phi™ Coprocessors
Highly-parallel Processing for Unparalleled Discovery

**Groundbreaking: differences**

- Up to 61 IA cores/1.2 GHz/ 244 Threads
- Up to 16GB memory with up to 352 GB/s bandwidth
- 512-bit SIMD instructions
- Linux operating system, IP addressable
- Standard programming languages and tools

**Leading to Groundbreaking results**

- Over 1.2 TeraFlop/s double precision peak performance
- Enjoy up to 1.79x higher memory bandwidth than on an Intel® Xeon® processor E5 family-based server.
- Up to 3x more performance per watt than with an Intel® Xeon® processor E5 family-based server.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

For more information go to [http://www.intel.com/performance](http://www.intel.com/performance)  Notes 1, 2 & 3, see backup for system configuration details.
**Intel® Xeon Phi™ Coprocessors: They’re So Much More**

*General purpose IA Hardware leads to less idle time for your investment*

### Restrictive architectures

- Custom HW Acceleration
- GPU
- ASIC
- FPGA

- Run restricted code

### It’s a supercomputer on a chip

- Operate as a compute node
- Run a full OS
- Program to MPI
- Run x86 code
- Run offloaded code

*Intel® Xeon Phi™ Coprocessor*

Restrictive architectures limit the ability for applications to use arbitrary nested parallelism, functions calls and standard threading models.

*Refer to [software.intel.com/mic-developer](http://software.intel.com/mic-developer) for details on the Intel Xeon Phi™ coprocessor*
## Intel® Xeon Phi™ Coprocessor Product Lineup

<table>
<thead>
<tr>
<th>Family</th>
<th>Description</th>
<th>Performance/$ leadership</th>
<th>16GB GDDR5</th>
<th>8GB GDDR5</th>
<th>6GB GDDR5</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 Family</td>
<td>Highest Performance Most Memory</td>
<td></td>
<td>352GB/s</td>
<td>&gt;300GB/s</td>
<td>240GB/s</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&gt;1.2TF DP</td>
<td>&gt;1TF DP</td>
<td>&gt;1TF DP</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>300W TDP</td>
<td>225-245W TDP</td>
<td>300W TDP</td>
</tr>
<tr>
<td>5 Family</td>
<td>Optimized for High Density Environments Performance/Watt leadership</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 Family</td>
<td>Outstanding Parallel Computing Solution</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Knights Landing: Next Generation Intel® Xeon Phi™ Product Family

- Designed using Intel’s cutting-edge 14nm Transistor Technology
- Not bound by “offloading” bottlenecks: Standalone CPU or PCIe Coprocessor
- Common instruction set architecture: Intel® Advanced Vector Extensions 512
- Leadership compute & memory bandwidth: Integrated on-package Memory
- Performance to drive new discovery: >3 teraFlops DP, >60 Cores, Improved Single Thread

14nm technology will deliver more compute density and power efficiency than any previous Intel process.¹

As a host processor, Knights Landing will deliver a leap in compute density, power efficiency & reliability.

Commonality & backward compatibility for future 512-bit instruction set architectures;

On-package memory will significantly increase memory bandwidth, delivering greater performance for memory-bound workloads

Compute capability to match the increased memory bandwidth, single thread performance² improves serial code sections.

² single threaded performance improvement over current generation Intel® Xeon Phi™ Coprocessors 7100, 5100, 3100 series products
Knights Landing Integrated On-Package Memory

**Cache Model**
Let the hardware automatically manage the integrated on-package memory as an “L3” cache between KNL CPU and external DDR.

**Flat Model**
Manually manage how your application uses the integrated on-package memory and external DDR for peak performance.

**Hybrid Model**
Harness the benefits of both cache and flat models by segmenting the integrated on-package memory.

Maximizes performance through higher memory bandwidth and flexibility\(^1\)

---

\(^1\) As compared with Intel® Xeon Phi™ x100 Coprocessor Family.

Diagram is for conceptual purposes only and only illustrates a CPU and memory – it is not to scale, and is not representative of actual component layout.
Consistent Tools, Programming Models & Optimization Techniques

```c
int main(int argc, char* argv[]) {
    // example code
    first_function();
    second_function();
    return 0;
}
```

Increasing Code Parallelism == Higher Performance
Wide Range of Development Options

Thread Parallelism

- Intel® Math Kernel Library
- MPI*
- OpenMP*
- Intel® Threading Building Blocks
- Intel® Cilk™ Plus
- Pthreads*

Vector Parallelism

- Intel® Math Kernel Library
- Auto-vectorization
- Semi-auto Vectorization (e.g. #pragma ivdep)
- Explicit Vectorization (e.g. Intel® Cilk™ Plus array notation)
- OpenCL*
- Intrinsics

Ease of Use

Fine Control
Illustrative example

Fortran code using MPI, single threaded originally. Run on Intel® Xeon Phi™ coprocessor natively (no offload).

Untuned Performance on Intel® Xeon® processor

Untuned Performance on Intel® Xeon Phi™ coprocessor

Based on an actual (but confidential) customer example. Shown to illustrate a point about common techniques. Your results may vary!
Illustrative example
Fortran code using MPI, single threaded originally.
Run on Intel® Xeon Phi™ coprocessor natively (no offload).

Based on an actual (but confidential) customer example.
Shown to illustrate a point about common techniques.
Your results may vary!
Illustrative example

Fortran code using MPI, single threaded originally. Run on Intel® Xeon® processor originally.

Run on Intel® Xeon Phi™ coprocessor natively (no offload).

Common optimization techniques...
“dual benefit”

Based on an actual (but confidential) customer example. Shown to illustrate a point about common techniques. Your results may vary!
Illustrative example

Fortran code using MPI, single threaded originally.
Run on Intel® Xeon Phi™ coprocessor natively (no offload).

Common optimization techniques...
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Based on an actual (but confidential) customer example.
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Your results may vary!

Untuned Performance on Intel® Xeon® processor
Untuned Performance on Intel® Xeon Phi™ coprocessor
TUNED Performance on Intel® Xeon® processor
TUNED Performance on Intel® Xeon Phi™ coprocessor
Key Considerations for Parallelism and Higher Performance for programmers to identify and use

**Vectorization (wider vectors)**

“Data parallelism”

**Scaling (more cores and more threads)**

“Task parallelism”

**Memory Usage**

“Locality and Alignment”
Parallelism in Modern Computer Architecture

Instruction-Level Parallelism (ILP)
- Pipelining
- Multiple instruction issue
- Out-of-Order execution

Vectorization (SIMD)
- Single instructions can be applied to more than one piece of data

Threading (MIMD)
- Multiple instances of a program can run simultaneously
Parallelism in Modern Computer Architecture

Instruction-Level Parallelism (ILP)
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- Multiple instruction issue
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Vectorization (SIMD)
- Single instructions can be applied to more than one piece of data

Threading (MIMD)
- Multiple instances of a program can run simultaneously
What is SIMD?

Scalar Code
- Executes code one element at a time.

Vector Code
- Executes code multiple elements at a time.
- Single Instruction Multiple Data.
Preparing Code for SIMD

Precision is important: impacts the SIMD width.

Identify Hotspots

Integer or FP?

FP

Integer

Can convert to SP?

Yes

Change to SP

No

Re-layout data for SIMD efficiency

Align data structures

Convert code to SIMD form

Follow SIMD coding guidelines

Optimize memory access patterns and prefetch (if appropriate)

Further optimization

精密性很重要：影响SIMD宽度。
Data Layout – Why It’s Important

Instruction-Level

- Hardware is optimized for contiguous loads/stores.
- Support for non-contiguous accesses differs with hardware. (e.g. AVX2/KNC gather)

Memory-Level

- Contiguous memory accesses are cache-friendly.
- Number of memory streams can place pressure on prefetchers.
# Data Layout – Common Layouts

## Array-of-Structs (AoS)

<table>
<thead>
<tr>
<th>x</th>
<th>y</th>
<th>z</th>
<th>x</th>
<th>y</th>
<th>z</th>
<th>x</th>
<th>y</th>
<th>z</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>y</td>
<td>z</td>
<td>x</td>
<td>y</td>
<td>z</td>
<td>x</td>
<td>y</td>
<td>z</td>
</tr>
</tbody>
</table>

- **Pros:**
  - Good locality of \{x, y, z\}.
  - 1 memory stream.

- **Cons:**
  - Potential for gather/scatter.

## Struct-of-Arrays (SoA)

<table>
<thead>
<tr>
<th>x</th>
<th>x</th>
<th>x</th>
<th>x</th>
<th>x</th>
<th>x</th>
<th>y</th>
<th>y</th>
<th>y</th>
</tr>
</thead>
<tbody>
<tr>
<td>y</td>
<td>y</td>
<td>y</td>
<td>y</td>
<td>y</td>
<td>y</td>
<td>z</td>
<td>z</td>
<td>z</td>
</tr>
</tbody>
</table>

- **Pros:**
  - Contiguous load/store.

- **Cons:**
  - Poor locality of \{x, y, z\}.
  - 3 memory streams.

## Hybrid (AoSoA)

<table>
<thead>
<tr>
<th>x</th>
<th>x</th>
<th>y</th>
<th>y</th>
<th>z</th>
<th>z</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td>y</td>
<td>y</td>
<td>z</td>
<td>z</td>
</tr>
</tbody>
</table>

- **Pros:**
  - Contiguous load/store.
  - 1 memory stream.

- **Cons:**
  - Not a “normal” layout.
Data Alignment – Why It’s Important

Cache Line 0

| 0 | 1 | 2 | 3 | ... | 6 | 7 |

Cache Line 1

| 0 | 1 | 2 | 3 | 6 | 7 | 8 | 9 |

Aligned Load
- Address is aligned.
- One cache line.
- One instruction.

Unaligned Load
- Address is not aligned.
- Potentially multiple cache lines.
- Potentially multiple instructions.
Scaling: OpenMP

OpenMP is used in a shared memory space

Often referred to as threading, allows multiple tasks to occur simultaneously which are:

- Embarrassingly parallel
- Are working in disjoint areas of memory
- Can have any “intersections” of threads be caught using atomic or critical sections

Diagrams courtesy of Lawrence Livermore Nat’l Lab

https://computing.llnl.gov/tutorials/parallel_comp/#MemoryArch
Scaling: MPI

MPI is used in a distributed memory space

Often referred to as message passing, allows multiple chunks of a problem’s domain to be computed on simultaneously

Each computer functions alone with the network acting as the bridges between to update values on process boundaries between iterations

Diagrams courtesy of Lawrence Livermore Nat’l Lab

https://computing.llnl.gov/tutorials/parallel_comp/#MemoryArch
MPI + OpenMP: Hybrid Scaling

The two paradigms can be used together

*Note: For maximum utilization of the Intel® Xeon Phi™ Coprocessor, multiple tasks/threads per core is almost always required.*

An example would be having a few MPI ranks on each coprocessor and then having many threads spawned by each rank

Diagrams courtesy of Lawrence Livermore Nat’l Lab

[https://computing.llnl.gov/tutorials/parallel_comp/#MemoryArch](https://computing.llnl.gov/tutorials/parallel_comp/#MemoryArch)
Utilizing an Intel® Xeon Phi™ Coprocessor (1/2)

Native
- Target Code: Highly parallel (threaded and vectorized) throughout.
- Potential Bottleneck: Serial/scalar code.

Offload
- Target Code: Mostly serial, but with expensive parallel regions.
- Potential Bottleneck: PCIe* data transfers.

Symmetric
- Target Code: Highly parallel and performs well on both platforms.
- Potential Bottleneck: Load imbalance.
Utilizing an Intel® Xeon Phi™ Coprocessor (2/2)

MPI*
- Used for “native” and “symmetric” execution.
- Can launch ranks across processors and coprocessors.

OpenMP*
- Used for “native”, “offload” and “symmetric” execution.
- Newest standard (4.0) supports “target” syntax for offloading.

Many real-life HPC codes use a native MPI/OpenMP hybrid
- Balance task granularity by tuning combination of ranks/threads. (e.g. 16 MPI ranks x 15 OpenMP threads)
Dual-Tuning Benefits

Single C/C++/Fortran source code will run on both platforms
- Same compiler, libraries and tools available across hardware.

The key difference between platforms is scale
- Both x86-based; both have SIMD; both have threads...
- Optimizations targeting one benefit the other.
- Coprocessor is more sensitive to parallelism, so benefits more.
Modern Computer Architecture
It’s about Parallelism

Summary

- Vectorize, Scale and Memory layout/locality are key to impressive performance gains
- Both Processor and Coprocessor benefits from parallel optimizations
  - Maintain a Single Source for current and future processing products
- Without parallelism, you’re severely limiting your maximum performance.
Application Performance Examples
# Intel® Xeon Phi™ Coprocessor: Increases Application Performance up to 7x

## Application/Code Performance vs. 2S Xeon*

<table>
<thead>
<tr>
<th>Segment</th>
<th>Application/Code</th>
<th>Performance vs. 2S Xeon*</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCC</td>
<td>NEC / Video Transcoding (see case study: <a href="#">NEC Case Study</a>)</td>
<td>Up to 3.0x²</td>
</tr>
<tr>
<td>Energy</td>
<td>Seismic Imaging ISO3DFD Proxy 16th order Isotropic kernel <strong>RTM</strong></td>
<td>Up to 1.45x³</td>
</tr>
<tr>
<td></td>
<td>Seismic Imaging 3DFD TTI 3- Proxy 8th order <strong>RTM</strong> (complex structures)</td>
<td>Up to 1.23x³</td>
</tr>
<tr>
<td></td>
<td>Petrobras Seismic ISO-3D <strong>RTM</strong> (with 1, 2, 3 or 4 Intel® Xeon Phi™ coprocessors)</td>
<td>Up to 2.2x, 3.4x, 4.6x or 5.6x⁴</td>
</tr>
<tr>
<td>Financial Services</td>
<td>BlackScholes SP / DP</td>
<td>SP: Up to 2.12x³; DP Up to 1.72x³</td>
</tr>
<tr>
<td></td>
<td>Monte Carlo European Option SP / DP</td>
<td>SP: Up to 7x³; DP Up to 3.13x³</td>
</tr>
<tr>
<td></td>
<td>Monte Carlo RNG European SP / DP</td>
<td>SP: Up to 1.58x³; DP Up to 1.17x³</td>
</tr>
<tr>
<td></td>
<td>Binomial Options SP / DP</td>
<td>SP: Up to 1.85x³; DP Up to 1.85x³</td>
</tr>
<tr>
<td>Life Science</td>
<td>BWA/Bio-Informatics</td>
<td>Up to 1.5x⁴</td>
</tr>
<tr>
<td></td>
<td>Wayne State University/MPI-Hammer</td>
<td>Up to 1.56x¹</td>
</tr>
<tr>
<td></td>
<td>GROMACS / Molecular Dynamics</td>
<td>Up to 1.36x¹</td>
</tr>
<tr>
<td>Manufacturing</td>
<td>ANSYS / Mechanical SMP</td>
<td>Up to 1.88x⁵</td>
</tr>
<tr>
<td></td>
<td>Sandia Mantevo / miniFE case study: <a href="#">software.intel.com/en-us/articles/running-minife-on-intel-xeon-phi-coprocessors</a></td>
<td>Up to 2.3x⁴</td>
</tr>
<tr>
<td>Physics</td>
<td>ZIB (Zuse-Institut Berlin) / Ising 3D (Solid State Physics)</td>
<td>Up to 3.46x¹</td>
</tr>
<tr>
<td></td>
<td>ASKAP ThogbomClean (astronomy)</td>
<td>Up to 1.73x⁴</td>
</tr>
<tr>
<td></td>
<td>Princeton / GTC-P (Gyrokinetic Toroidal) Turbulence Simulation IVB</td>
<td>Up to 1.18x⁶</td>
</tr>
<tr>
<td>Weather</td>
<td>WRF / Code WRF V3.5</td>
<td>1.56x⁶</td>
</tr>
</tbody>
</table>

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1. 25 Xeon E5 2670 vs. 25 Xeon* E5 2670 + 1 Xeon Phi® coprocessor (Symmetric)
2. 25 Xeon E5 2670 vs. 25 Xeon E5 2670 + 2 Xeon Phi™ coprocessor
3. 25 Xeon E5-2697v2 vs. 1 Xeon Phi™ coprocessor (Native Mode)
4. 25 Xeon E5-2697v2 vs. 25 Xeon E5 2697v2 +1 Xeon Phi™ coprocessor (Symmetric Mode) (for Petrobras, 1, 2, 3 or 4 Xeon Phi in the system)
5. 25 Xeon E5 2670 vs. 25 Xeon* E5 2670 + 1 Xeon Phi® coprocessor (Symmetric) (only 2 Xeon cores used to optimize licensing costs)
6. 4 nodes of 25 E5-2697v2 vs. 4 nodes of ES-2697v2 + 1 Xeon Phi™ coprocessor (Symmetric)

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Financial Services Workloads vs. NVIDIA® K40

Higher is better

Relative Performance

Financial Services Workloads

- Black-Scholes
- Monte Carlo Simulation DP
- Monte Carlo Simulation SP
- Monte Carlo RNG DP
- Monte Carlo RNG SP
- Binomial Options DP
- Binomial Options SP

Intel® Xeon Phi™ Coprocessor 7120A (16GB, 1.238 GHz, 61 core)
NVIDIA® K40, 2880 SP cores, 960 DP Cores, 745MHz (nominal) 875MHz Boost, 12GB Memory
Performance Proof-Point: Production Protein Sim. 474K Atoms

LAMMPS

- **Application**: LAMMPS
- **Description**: Simulation of Molecular Systems with Classical Models
- **Availability**: Target for 2014 Q3 Open Source Release
- **Usage Model**: Load balancer offloads part of neighbor-list and non-bond force calculations to Xeon Phi™ for concurrent calculations with CPU.
- **Highlights**: Dynamic load balancing allows for concurrent 1) data transfer between host and coprocessor, 2) calculations of neighbor-list, non-bond, bond, and long-range terms, and 3) some MPI communications
  - Same routines in LAMMPS Intel Package run faster on CPU
- **Results**: Simulation rate with Xeon Phi™ Offload is up to 1.5X when compared to optimized version running on CPU
- **Code Optimization Strategy**: Offload API used to run calculations well suited for many-core chips on both the CPU and the coprocessor
  - Same C++ routine is run twice, once with an offload flag, to support concurrent calculations
  - Standard LAMMPS "fix" object manages concurrency and synchronization
  - Adds support for single, mixed, and double precision calculations on both CPU and coprocessor
  - Vectorization (AVX on CPU / 512-bit vectorization on Phi™)

- **2S Intel® Xeon® processor E5-2697v2 (LAMMPS Baseline)**
- **2S Intel® Xeon® processor E5-2697v2 (LAMMPS IA Package)**
- **2S E5-2697v2 + Intel® Xeon Phi™ coprocessor 7120A Turbo Off (pre-production HW/SW)**

**Speedup (Mixed Precision)**
(Higher is Better)

<table>
<thead>
<tr>
<th></th>
<th>1 Node</th>
<th>32 Nodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.23</td>
<td>1.12</td>
</tr>
<tr>
<td>1.73</td>
<td>1.57</td>
<td></td>
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Embree Ray Tracing Kernels

Embree: Optimized Ray Tracing Toolkit

- High fidelity visualization toolkit for application developers
- Easy to integrate, rapid prototyping
- Highly efficient and scalable Ray Tracing features and capabilities
- Compatible with present and future compute platforms
- Available as Open Source on http://embree.github.com (Apache 2.0 license)
Embree Ray Tracing Performance

- Performance in rays per second for a 1920 x 1080 pixel image
- Dual socket Intel® Xeon® E5-2690 (16 cores total, 2.9GHz clock)
- Intel® Xeon Phi™ 7120 (61 cores, 1.28GHz clock)
- Embree 2.2 compiled with Intel Composer XE 14.0.1 and ISPC 1.6.0

<table>
<thead>
<tr>
<th>Scene</th>
<th>Primary Rays (higher is better)</th>
<th>Full Path Tracing (higher is better)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Xeon</td>
<td>Xeon Phi</td>
</tr>
<tr>
<td>Headlight</td>
<td>0.8M Tris</td>
<td>210M</td>
</tr>
<tr>
<td>Bentley</td>
<td>2.3M Tris</td>
<td>284M</td>
</tr>
<tr>
<td>Crown</td>
<td>4.8M Tris</td>
<td>349M</td>
</tr>
<tr>
<td>Dragon</td>
<td>7.4M Tris</td>
<td>234M</td>
</tr>
<tr>
<td>Power Plant</td>
<td>12.7M Tris</td>
<td>62M</td>
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</table>
Embree Performance versus OptiX

<table>
<thead>
<tr>
<th>Scene</th>
<th>Start Up Time (lower is better)</th>
<th>Rendering (higher is better)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Xeon</td>
<td>Xeon Phi</td>
</tr>
<tr>
<td>Headlight</td>
<td>0.8M Tris</td>
<td>0.1s</td>
</tr>
<tr>
<td>Bentley</td>
<td>2.3M Tris</td>
<td>0.3s</td>
</tr>
<tr>
<td>Crown</td>
<td>4.8M Tris</td>
<td>0.5s</td>
</tr>
<tr>
<td>Dragon</td>
<td>7.4M Tris</td>
<td>0.7s</td>
</tr>
<tr>
<td>Power Plant</td>
<td>12.7M Tris</td>
<td>1.3s</td>
</tr>
</tbody>
</table>

- Performance in seconds and rays per second for a 1920 x 1080 pixel image
- Startup time includes memory allocation, BVH build, data upload over PCI
- Dual socket Intel® Xeon® E5-2690 (16 cores total, 2.9GHz clock)
- Intel® Xeon Phi ™ 7120 (61 cores, 1.28GHz clock, 16 GB RAM)
- NVIDIA GeForce GTX Titan (6 GB RAM)
- Embree 2.2 compiled with Intel Composer XE 14.0.1 and ISPC 1.6.0
- OptiX version 3.5.1 built with CUDA 5.5
Hybrid OpenMP/MPI generalising CAMB for non-Gaussian theories
Part of key non-Gaussian pipeline for Planck satellite data analysis
Repeated integrations of early and late-time basis functions (2D Gauss-Legendre)

Key improvement - unrolling loops to allow auto-vectorization (7x speed-up on Coprocessor)

<table>
<thead>
<tr>
<th>Stage</th>
<th>2x Xeon Time (s)</th>
<th>2x Xeon Speed-up</th>
<th>MIC Time (s)</th>
<th>MIC Speed-up</th>
<th>MIC vs 2x Xeon Speed-up</th>
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</table>

Timescales:
3x on processor from loop unrolling, data align. = 1 hour
2x on coprocessor from OpenMP = 1 week

Single coprocessor performance equiv. of 4.5 processors
MODAL Addendum: Precomputed algorithm!

During optimisation, identified repetition
- can precompute array of size 1GB
- not obvious but quick implementation

730x speed-up over optimised 2 processors
4600x speed-up over original coprocessor

Observation V: Why think? We have computers to do that for us.
Or: Work smarter not harder (get programmer support)
A Growing Ecosystem:
Developing today on Intel® Xeon Phi™ coprocessors

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Intel® Parallel Computing Centers (IPCCs)

- Collaborations with universities, institutions, and labs
- Deliver Open, Standard, Portable, Scalable community codes and parallel programming training
- 15-20 Announced Worldwide
- More to come...
Questions?

To Learn more:

See CUG 2014 Tutorial 1B+2B materials and hands-on optimization labs

http://software.intel.com/mic-developer

...
## Intel® Xeon Phi™ Coprocessor x100 Family Reference Table

<table>
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<th>Processor Brand Name</th>
<th>Codename</th>
<th>SKU #</th>
<th>Form Factor, Thermal</th>
<th>Board TDP (Watts)</th>
<th>Max # of Cores</th>
<th>Clock Speed (GHz)</th>
<th>Peak Double Precision (GFLOP)</th>
<th>GDDR5 Memory Speeds (GT/s)</th>
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<th>Memory Capacity (GB)</th>
<th>Total Cache (MB)</th>
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*Available as part of a Xeon Phi™ starter kit only. Please see the Intel Xeon Phi™ Starter Kit Program (CDI doc# 539389) for SKU details, and [http://software.intel.com/en-us/xeon-phi-starter-kit](http://software.intel.com/en-us/xeon-phi-starter-kit) for OEMs offering the Starter Kits.

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Claim based on calculated theoretical peak double precision performance capability for a single coprocessor. 16 DP FLOPS/clock/core
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1. Peak DP FLOPS claim based on calculated theoretical peak double precision performance capability for a single coprocessor. 16 DP FLOPS/clock/core * 61cores * 1.238GHz = 1.208TeraFlop/s.

2. Memory Bandwidth: 2 socket Intel® Xeon® processor E5-2600v2 product family server vs. Intel® Xeon Phi™ coprocessor (1.79x: Measured by Intel Q4 2013. 2 socket E5-2687v2 (12 core, 2.6GHz) vs. 1 Intel® Xeon Phi™ coprocessor 7120P (61 cores, 1.238GHz) on STREAM Triad benchmark 101 GB/s vs. 181GB/s ) (TR1364 & TR2039C)

3. Performance/Watt: 2 socket Intel® Xeon® processor E5-2697v2 server vs. a single Intel® Xeon Phi™ coprocessor 5120D (60 cores, 1.053GHz) (Intel Measured DGEMM perf/watt score 548.13GF/s @ 451W vs. 837.43 GF/s @ 225W) (TR 1390 & TR 2039C)
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