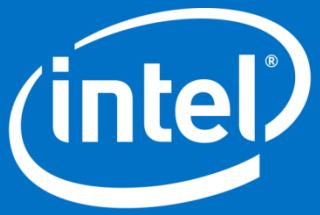


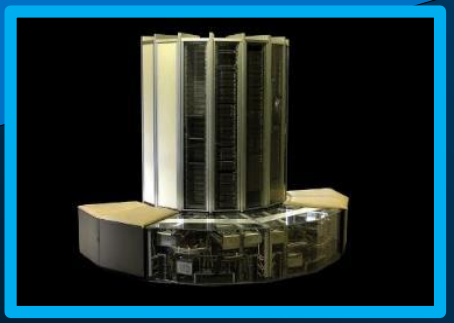
Changing Needs/Solutions/Roles

Rajeeb Hazra

Vice President, Data Center Group
General Manager, Enterprise & High Performance Computing Platforms
Intel Corporation

Three Decades of High Performance Computing

Vertically integrated



Cray - 1 (1975)
250 MFLOPS

- Fewer fast proprietary processors
- Custom software
- ~$5-8M System Cost
- Government labs

Massively Parallel

Connection Machine - 2 (1987)
2.5 GFLOPS

- Unix, VMS and proprietary programming models
- ~$5M System Cost
- Scientific & Commercial

Democratized HPC

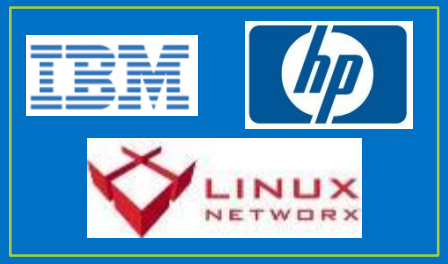
Beowulf Cluster (1996)
1+ GFLOPS

- Commodity compute, network, & storage
- Standard Linux & parallel programming models
- ~$50K System cost
- Government Labs, Academia & Commercial

Intel's Role: The x86 "Ecosystem"

The Past: '00-'05

Ad Hoc: Few, incompatible HPC system vendors



Intel: supply silicon

The Present: '06-Today

ICR Platform Spec: ecosystem of many compatible system & apps

Specification delivered to

Intel: enable interoperability

Is the Future More of the Present?

The Writing On The Wall

Technology Disruptions

Integration

Storage
Re-architecture

Software Transformation

Increased Demand

New users & usages …
Cloud makes HPC more accessible

PayPal™

Real-time analytics using HPC

Intensified Competition

OpenPOWER™

ARM®

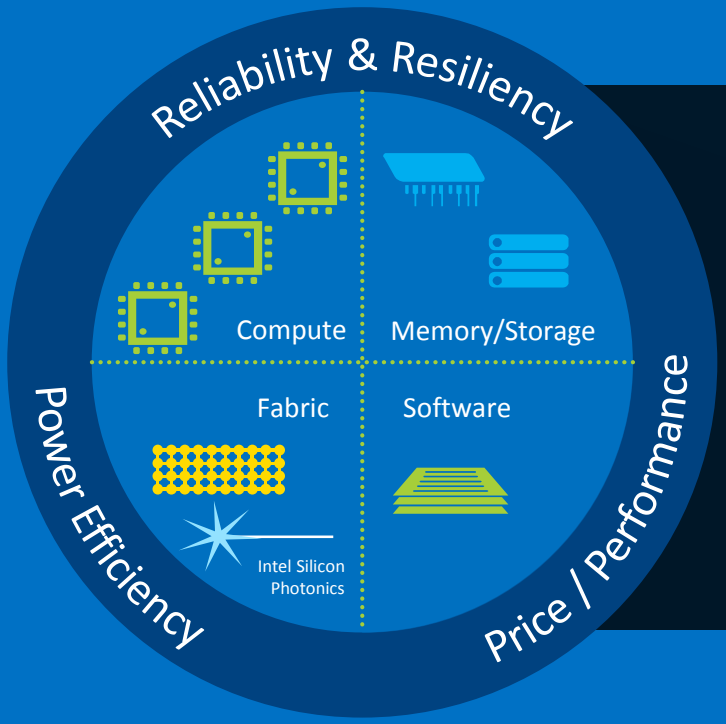
Indigenous
CPU interests

Channel Challenges

Increasing complexity
Software Fragmentation
Differentiation
New market makers

Intel's HPC Scalable System Framework (SSF)

A design foundation enabling wide range of highly workload-optimized solutions



Small clusters to Supercomputers

Compute and Data-Centric Computing

Standards-Based Programmability

Intel® Xeon® Processors
Intel® Xeon Phi™ Coprocessors
In Package Memory

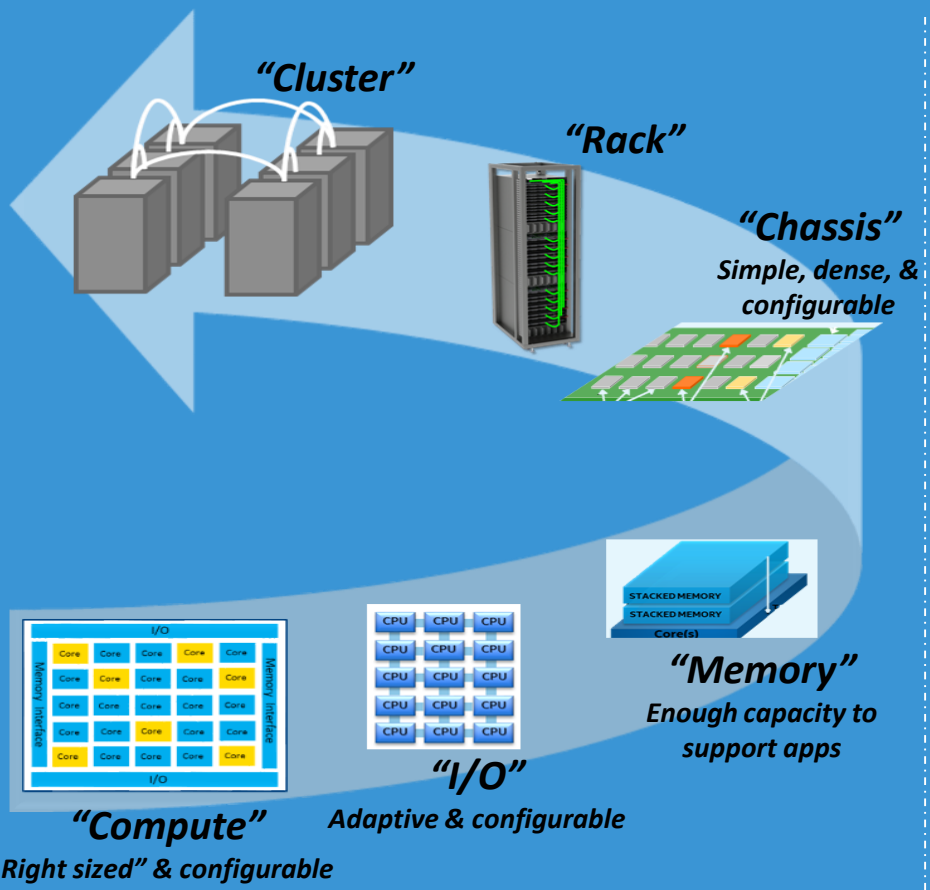
Intel® True Scale Fabric
Intel® Omni-Path Fabric
Intel® Ethernet
Intel® Silicon Photonics Technology

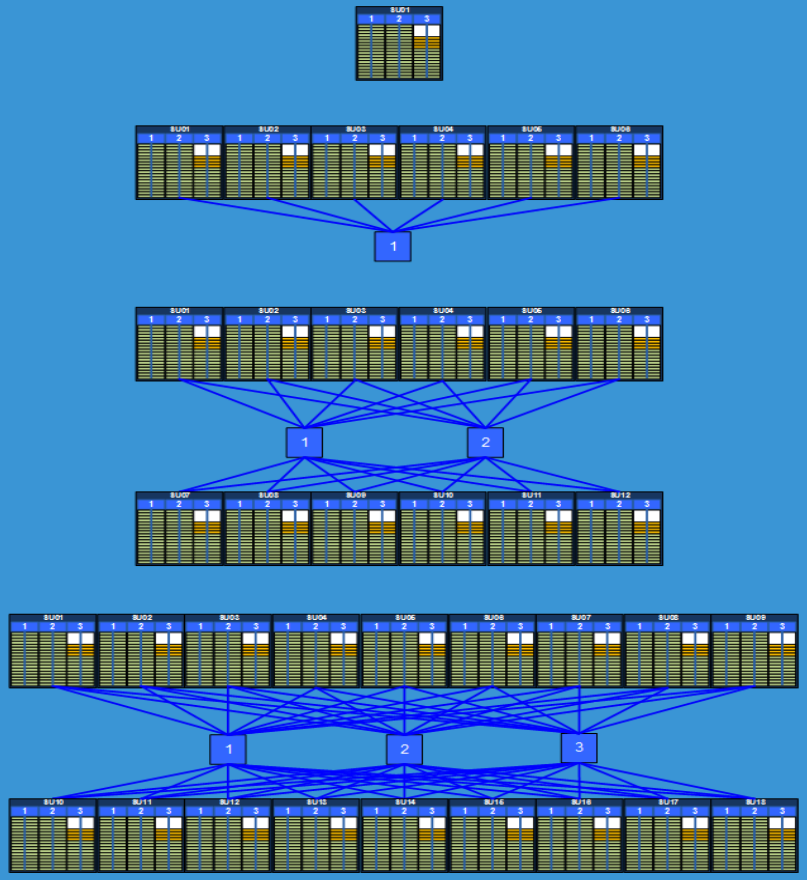
Next-generation NVM
Intel® SSDs
Intel® Lustre*-based Solutions

Intel® Sofware Tools
Intel Cluster Software

SSF: Enabling Configurability & Scalability

from components to racks to clusters



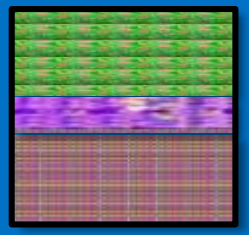


- Intel Xeon or Xeon Phi processors based on workloads
- Compute flexibly aggregated
- Low latency compute to compute interconnect

- I/O Topologies for high performance
- Configurable I/O bandwidth director switch
- Burst buffer to decouple storage from I/O

SSF: Accommodating New Compute Paradigms

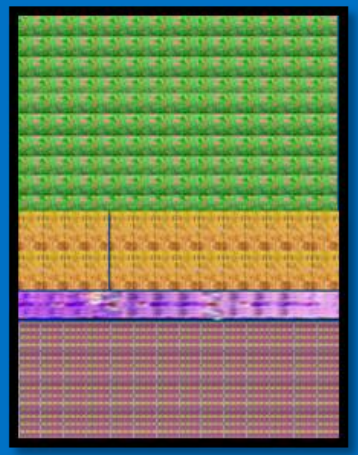
Today



Multi-Core

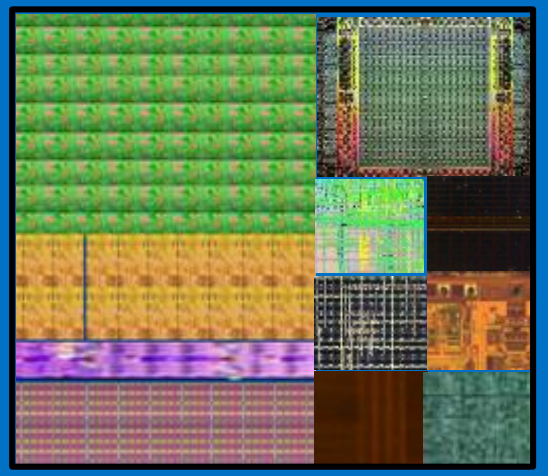
Many-Core

Next



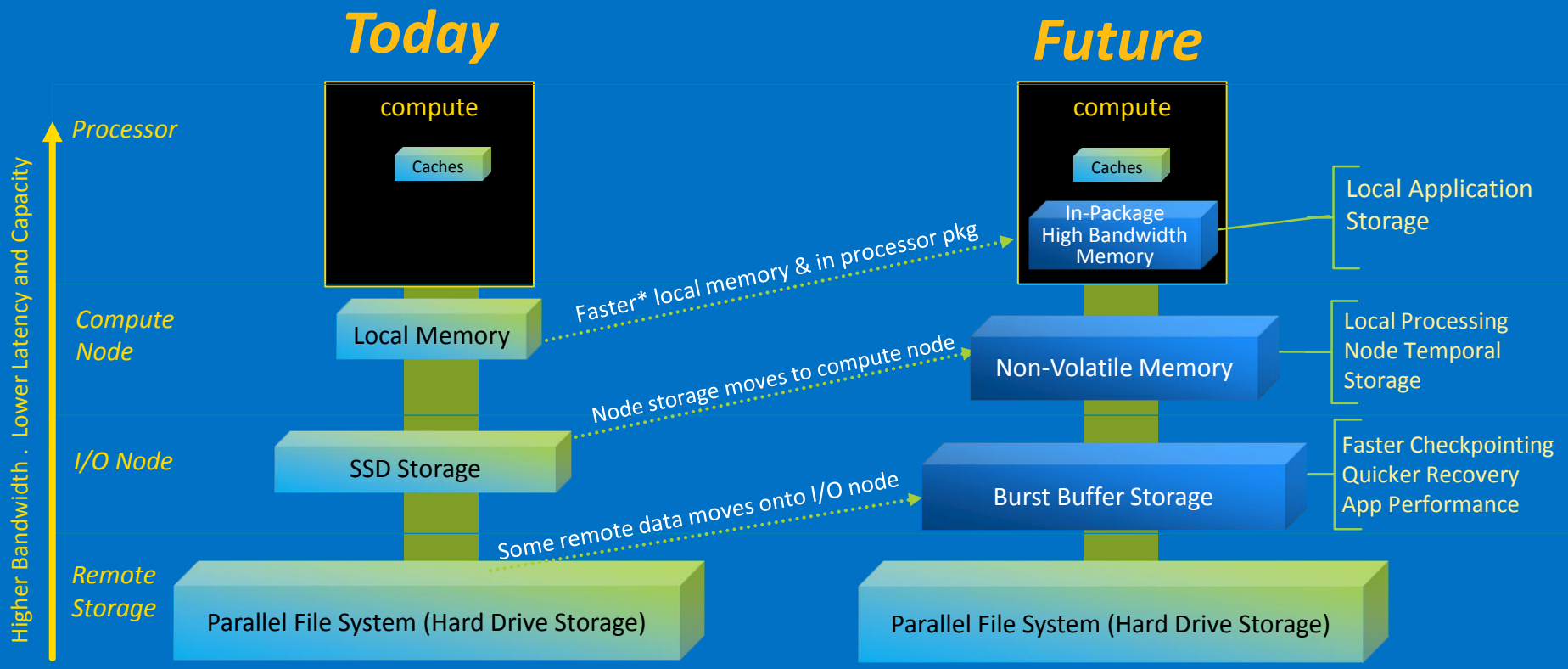
Integrating
Mixed Cores

The Future



Integrating
FPGA, Accelerators….

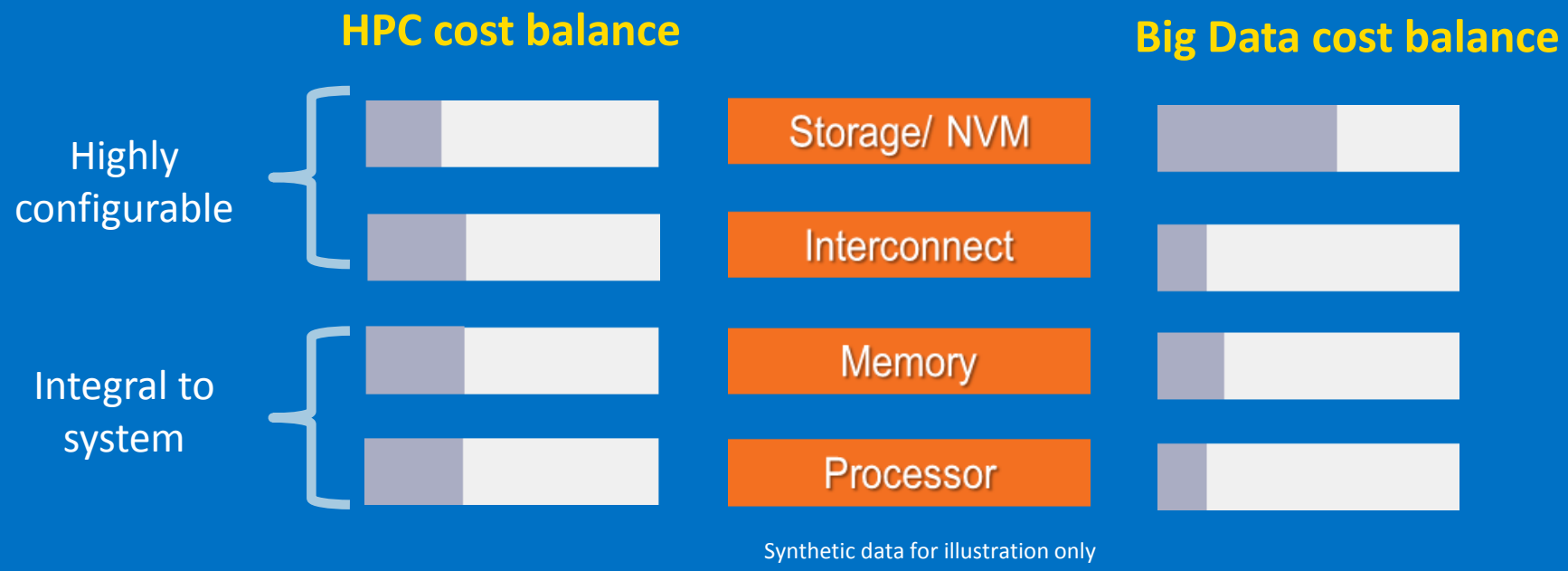
SSF: Re-architecting The Memory-Storage Hierarchy



Better data-intensive app performance and energy efficiency

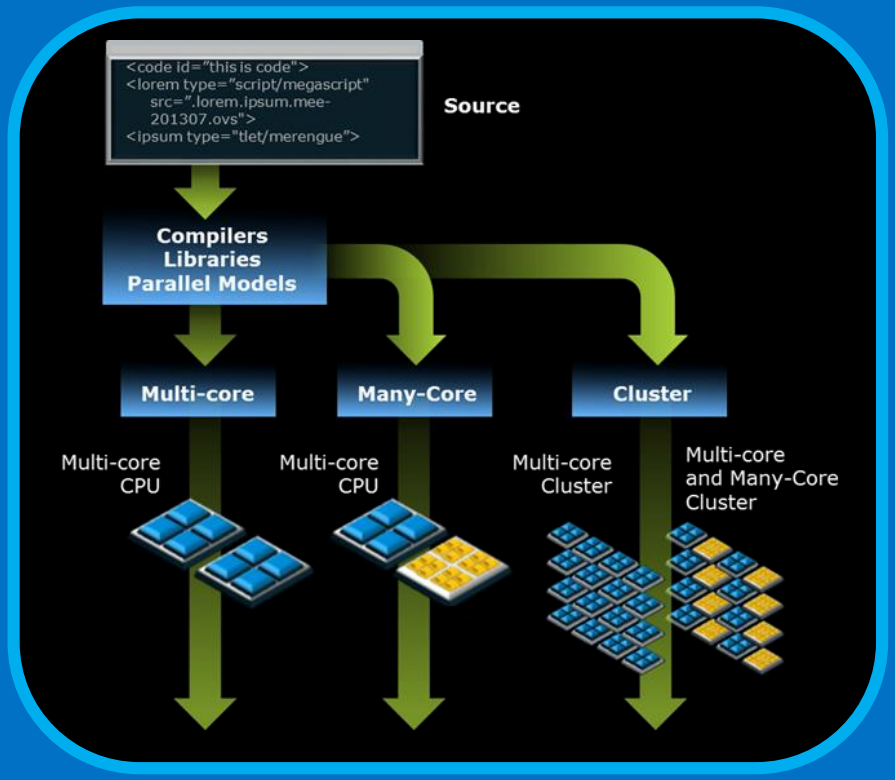
*Compared to standard DDR memory

SSF: End The "Big Data vs. HPC" Debate



A single, broadly configurable, framework to meet both requirements from a hardware perspective

SSF: Enabling A Single Programming Model



Instruction Parallelism	Data Parallelism	Thread Parallelism	Cluster / Process Parallelism

Serial Code

Fast Scalar performance, Optimized C/C++,FORTRAN, Threading and Performance Libraries, Debug / Analysis Tools

Parallel Node Level

Multi-core, Multi-Socket, SSE and AVX instructions, OpenMP, Threading and Performance Libraries, Thread Checker , Ct

Multi-Node / Cluster Level

Cluster Tools, Cluster OpenMP, MPI Checker

Unlike accelerators, optimizations for Intel® Xeon Phi™ and Intel® Xeon® products share the same languages, directives, libraries, and tools

Modernizing Community Codes

Together With You

Intel Parallel Computing Centers

50+ Centers
14 countries
80+ codes

Heading To The Era of SSF

ANL selected Intel and Cray for Extreme Scale HPC

Cori
NERSC‡
>30PF

April ’14

Trinity
NNSA†
>40PF

July ’14

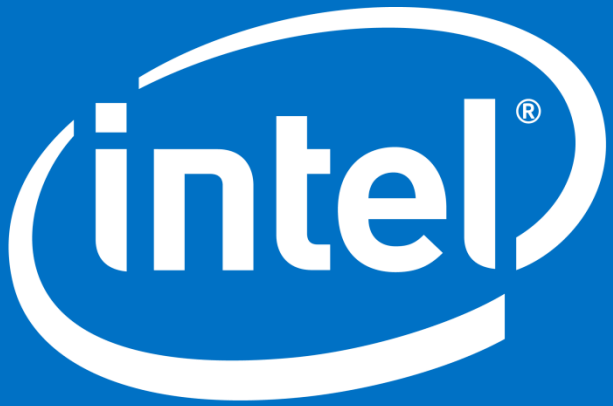
Aurora
Argonne National Laboratory
>180PF
CRAY
April ‘15

+

Theta
Argonne National Laboratory
>8.5PF

>$200M

‡ Cray XC Series at National Energy Research Scientific Computing Center (NERSC).
† Cray XC Series at National Nuclear Security Administration (NNSA).
*Other names and brands may be claimed as the property of others.



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